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Current-controlled grounded memristor emulator circuit based on analog multiplier

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Abstract: This paper proposes a current-controlled grounded memristor emulator circuit based on single four-quadrant analog multiplier, a resistor and a capacitor. The behavioral model of the proposed emulator circuit is analyzed, highlighting its characteristics. Experimental results are given to investigate its ability for different operating frequencies and they are in accordance with theoretical analysis and simulation results. By using a divider circuit, the memristance variation in the time domain is obtained. It is observed that the pinched hysteresis loop at high frequency loses symmetry due in part to the shift that introduces a multiplication of sinusoidal signals.

Keywords: Current-controlled memristor, pinched hysteresis loop, four-quadrant analog multiplier.

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1. Introduction

Since Chua´s introduced the memristor element (Chua, 1971) and Hewlett Packard made it using a thin film of titanium dioxide in 2008 (Strukov et al., 2008), this passive two-terminals element has widely been researched in order to be used in several real applications. Its characteristics of non-linearity and memory have made possible its use in analog-digital, neuromorphic and chaotic circuits mainly. The modeling of the memristor device has focused on macromodels generated with programming tools, and emulators which are used in different applications simulating the voltage-current behavior required. Memristor emulators have some advantages such as: the control of the memristance and operation frequency, as well as its functional availability at lower cost.

Due to non-linear behavior of memristors, active circuit elements provide advantages for the design of emulators. Various active circuit element based memristor circuits can be found in literature based on operational amplifier (OpAmp) (Kim et al., 2012), differential difference current conveyors (DDCC) (Yesil & Kuntman, 2014; Yener & Kuntman 2014), second-generation current conveyor (CCII) (Cam & Sedef, 2017; Sánchez et al., 2014; Sánchez et al., 2015; Sánchez & Aguila, 2017), operational transconductance amplifier (OTA) (Babacan et al., 2017; Babacan et al., 2016; Babacan & Kaçar, 2017; Yesil, 2019) differential voltage current conveyor transconductance amplifier (DVCCTA) (Ranjan et al., 2017), current backward transconductance amplifier (CBTA) (Ayten et al., 2017), current feedback operational amplifier (CFOA) (Abuelma'Atti & Khalifa, 2014; 2015). However, in all cases, active devices have been reported as the heart of the designs, but they are generally accompanied by additional ones, such as multipliers, or several of the same devices connected in cascade. Some reports whose tendency is to use a single active device, in the end include extra multipliers (Ayten et al., 2017; Yesil et al., 2014) or assemble functions presenting them as a single active device and they use two commercial devices for their physical implementation (Ranjan et al., 2017). To the authors' knowledge, the only report to date that actually uses a single active device is (Yesil et al., 2019), where a voltage difference transconductance amplifier (VDTA) with minimal external elements generates a memristor emulator circuit. With this perspective this paper presents a circuit that generates the voltage output of a current-controlled memristor with the help of an AD633JN multiplier, moreover, with an additional divider implemented with the same active circuit we get the value of the memristance. Comparing the performance of this device with an emulator circuit, the main difference is that it can not strictly replace the memristor itself, since in this case there are three terminals where one necessarily goes to ground, another establishes a current in an RC circuit and the output is the expected voltage between its terminals, emulating the behavior of a current-controlled grounded memristor. Through some changes in the capacitor voltage connections, taking advantage 4-quadrant multiplication, it is possible to implement both incremental and decremental modes. The use of a complex function such as that of the multiplier has the advantage that the emulation is achieved with a single integrated circuit, with a minimum of external components and the current can be adjusted to a magnitude greater than that reported with another single device (Yesil et al., 2019).

Analyzing its properties, it verifies that its frequency response is limited by operating frequency of the multiplier circuit, as well as by the phase shift associated with its operation. An advantage is that the voltages used in the product operation are determined by an RC circuit, so it is relatively easy to choose the RC values that set a desirable current at a certain frequency, whose only restriction would be to not exceed the maximum allowable voltages to be multiplied.

In this paper the memristive emulation based on multiplier is introduced, its behavioral model is derived highlighting some of its properties, HSPICE simulations are presented. The theoretical derivation is validated through practical implementation by using commercially available device AD633JN multiplier, finally, the conclusion is summarized in Section 5.

2. Memristive emulation

The memristive emulation consists of single AD633JN (Data Sheet AD633JN) as an active element and a serial resistor-capacitor arrangement as shown Fig.1(a). The output voltage is defined as

$$W_1 = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_1 \quad (1)$$

where the potential difference between X_1 and X_2 is the voltage at the capacitor denoted as $V_C = \frac{1}{C_1}\int i_{in}dt$ and between Y_1 and Y_2 is the voltage at the resistor defined as $V_R = R_1 i_{in}$. Furthermore, the potential at the input Z_1 is the same as the resistance so W_1 remains defined as

$$W_1 = \frac{V_R V_C}{10} + V_R = \frac{i_{in}R_1}{10C_1}\int i_{in}dt + i_{in}R_1 \quad (2)$$

By exchanging the terminals X_1 and X_2 on the capacitor the decremental memristance can be obtained, this due to differential X and Y inputs. The connection points for incremental

and decremental modes are shown in Fig.1(b). Since the current-controlled memristance is defined as $R_M = v(t)/i(t)$ and considering that $v(t) = W_1$, it can be clearly seen from Eq.(2) that

$$R_M = R_1 \pm \frac{R_1}{10C_1}\int_0^t i_{in}(\tau)d(\tau) \quad (3)$$

Adding another AD633JN in divider configuration as shown in Fig. 2, you get the memristance $R_M = M(q)$ directly. Since the transfer function for the divider (Data Sheet AD633JN) is

$$Y_1 = -\frac{10W_1}{X_1} = -\frac{10(\frac{i_{in}R_1}{10C_1}\int i_{in}dt + i_{in}R_1)}{X_1} \quad (4)$$

Considering that

$$X_1 = -\frac{R_3}{R_2}Z_1 = -\frac{R_3}{R_2}i_{in}R_1 \quad (5)$$

and taking into account that $-\frac{R_3}{R_2} = -\frac{10}{R_1}$, then

$$Y_1 = R_M = M(q) = \frac{R_1}{10C_1}\int i_{in}dt + R_1 \quad (6)$$

3. System properties

Modeling the previous behavior with the following equation

$$y(t) = ax(t) + bx(t)\int_0^t i_{in}(\tau)d(\tau) \quad (7)$$

where a and b are scaling constants. Considering sinusoidal excitation and trigonometric identities, i.e. when $x(t) = k\,sin(wt)$, we obtain

$$\int_0^t i_{in}(\tau)d(\tau) = -\frac{k}{w}cos(wt) = \mp(\frac{1}{w})\sqrt{(k^2 + x(t)^2)} \quad (8)$$

Then (7) can be expressed as

$$y(t) = ax(t) + (-\frac{bx(t)}{w}\sqrt{(k^2 + x(t)^2)}) \quad (9)$$

The properties of this last equation are

- The first order equation $y(t)=ax(t)$ generates a line of symmetry.
- A pinched double-loop intersects itself in the pinch-point $(x_p,y_p) = (0, 0)$.

The double-loop pass by the boundary points $k(\pm1,\pm a)$.

- The total area of the two lobes of the pinched hysteresis is given by $A = (4bk^3)/3w$.
- The relation $(y(t))/(x(t))$ that defines the memristance assuming that $x(t) = kSin(wt)$ could be expressed as $(y(t))/(x(t)) = a \mp \frac{bk}{w}\cos(wt)$.

Comparing (9) with (2), we observe that $y(t) = v_{out}(t)$, $x(t) = i_{in}(t)$,$a = R_1$ and $b = R_1/10C_1$ so the area and memristance would be respectively $A = R_1k^3/15C_1\pi f$ and $M(q) = R_1 \mp (R_1k/20C_1\pi f)cos(wt)$. As can be see, the memristance is composed by a linear time-invariant resistor and a linear time-varying resistor, and whether the frequency of the exciting source increases to infinity, entail that the linear time-varying resistor will reduce to zero.

The relationship between both parts may as well be described by the ratio of their amplitudes, given as

$$\gamma = \frac{k}{20C_1\pi f} = \frac{1}{\tau f} = \frac{T}{\tau} \quad (10)$$

where $\tau = (20C_1\pi f)/k$ is the time constant of the emulator circuit and $T = 1/f$ is the period of $i_{in}(t)$. Note that for holding the frequency-dependent pinched hysteresis loop τ must be updated according to f and only C_1 can be used for this task assuming that the amplitude of the current signal source k is constant. Furthermore, (10) also reveals that

a) $\gamma \to 0$ when $f \to \infty$ and the memristor behavior becomes dominated by its linear time-invariant part.
b) $\gamma \to 1$ when $f \to 1/\tau$ and the maximum pinched hysteresis loop is achieved.
c) $\gamma \to \geq 1$ when $f \to \leq 1/\tau$ and the hysteresis loop is lost.

Considering that the time-variant part is responsible for preserving the pinched-hysteresis which declines with increased frequency can be observed in the literature (Abuelma'Atti & Khalifa, 2014; Babacan et al., 2017; Kim et al., 2012; Sánchez et al., 2014; Yesil et al., 2014) that there is an inverse relationship with the product of resistive-capacitive elements and capacitive elements only, that can be represented in general as $wR_eq\,C$ (Abuelma'Atti & Khalifa, 2014; Kim et al., 2012; Sánchez et al., 2014) and wC (Babacan et al., 2017; Yesil & Kuntman, 2014), respectively. It is clear that those who handle the wC product preserve the pinched hysteresis loop at higher frequencies, as in the case of this paper. However here the frequency response is limited by the proposed device, although it is possible to increase the bandwidth with another multiplier, for instance the HA-2556 reports up to 52 MHz of bandwidth and with differential inputs Vx, Vy and Vz could even be possible to achieve a floating version of the memristive emulator circuit.

4. Experimental results and simulations

The circuit in the Fig. 1 was built on the breadboard using the AD633JN multiplier commercially available. Values of passive elements C_1=100 nF and R_1= 1 kΩ are chosen to work at $0<\gamma<1$ in order to hold frequency-dependent pinched hysteresis loop

behavior. The supply voltages are chosen as ±15 volts and we applied 5V sinusoidal voltage at 500 Hz, 1 kHz, 5 kHz and 10 kHz where the voltage in R_1 has been used to indirectly plot $i_{in}(t)$. Fig. 3 shows the pinched hysteresis loops to the mentioned frequencies so they become dominated by their linear time-invariant resistor according to the frequency increments, confirming the theory. Note that the Y-axis in Fig. 3 is the voltage $v_{out}(t)$ of the AD633JN. The numerical values of the discrete components C_1 and R_1 above were also used in the experimental and simulation tests of the decremental topology a 1 kHz shown in Fig. 4. In order to show its performance at higher frequencies and preserving the τ value mentioned above, a value of C_1= 150 pF was chosen, obtaining the double loops graphs shown in Fig. 5. As already mentioned in previous reports (Elwakil et al., 2013; Sánchez et al., 2015; Yang et al., 2015), the offset and nonsymmetrical pinched hysteresis loop is common at high frequencies which can be seen in Figs. 5(a),5(b),5(c) and 5(d). To explain these variations has been mentioned the presence of parasitic elements (Elwakil et al., 2013; Yang et al., 2015) and integrator nonidealities (Sánchez et al., 2015). We could corroborate that there is a phase shift between $i_{in}(t)$ and v_{out}(t) associated with the operation of multiplication and sum of the AD633JN which degenerates into Lissajous figures at higher frequencies. This is evidenced in Fig. 6 where the pinched hysteresis loop has disappeared at 500 kHz with the same values of capacitance and resistance above. A better study that is beyond the purpose of this paper will be necessary to detail the behavior of the loop at higher frequencies under this design proposal. Another characteristic behavior of memristor is the nonvolatility which can be observed in the capacitor voltage V_C, moreover, memristance changes could theoretically be seen in the node M(q) of Fig. 2. However, in (4) we can see that the division could give us errors if X1 takes values of zero as it would happen if we applied input pulses. Therefore, only the HSPICE simulation is shown for a pulse train at 25 kHz with 0.4 V of amplitude and 20µs pulse width in Fig. 7. Because the memristance is composed of a linear time-invariant resistor (in this case 1 KΩ) and a linear time-varying resistor the initial value it takes is the negative saturation of the OPAMP from which it begins to vary until reaching the positive saturation. The behavior of the simulated and experimental capacitor voltage V_C is shown in Fig. 8.

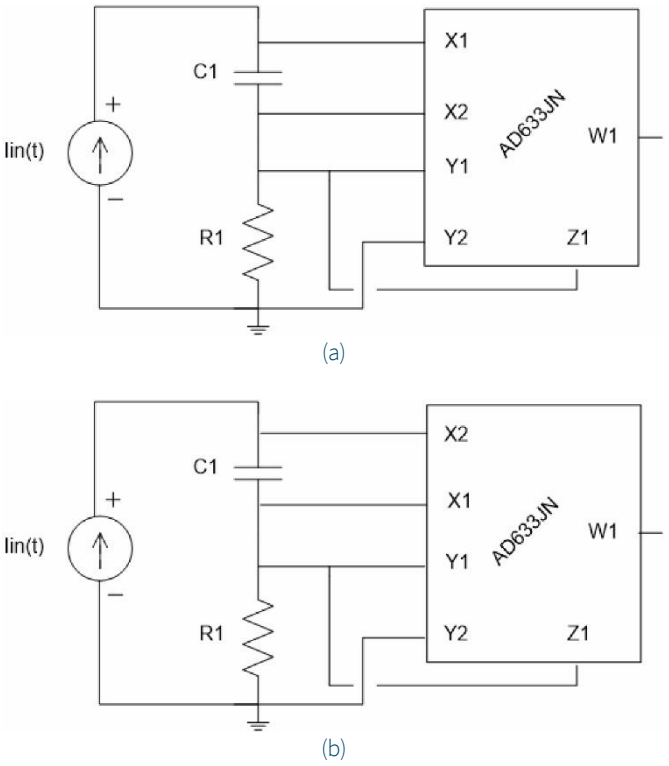


Figure 1. Memristor emulator circuit based on AD633JN: (a) Incremental topology, (b) Decremental topology.

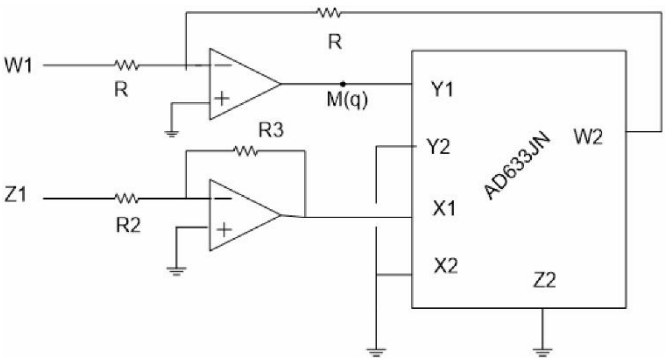
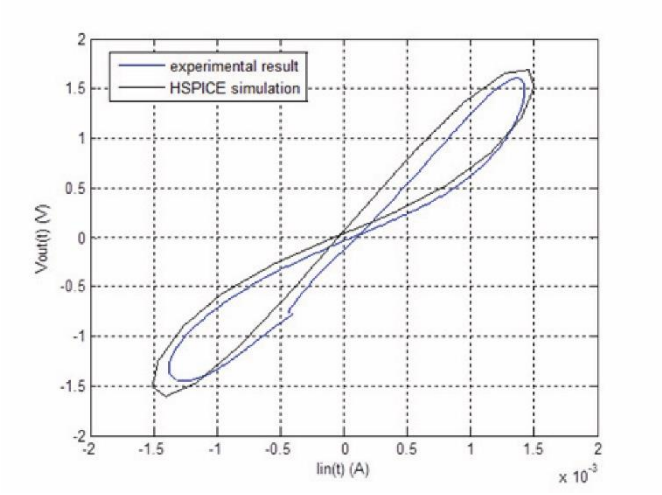
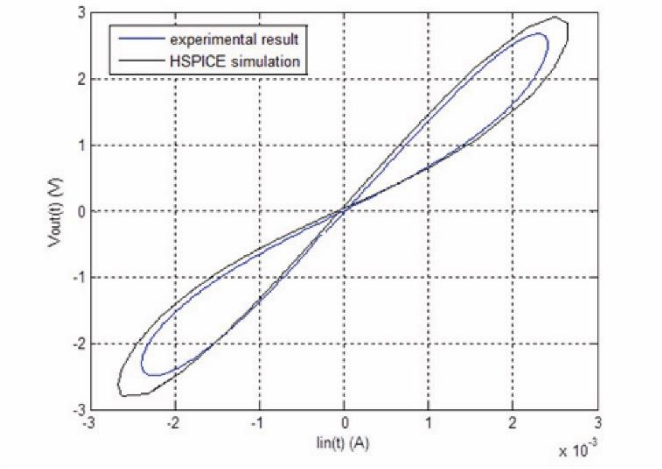


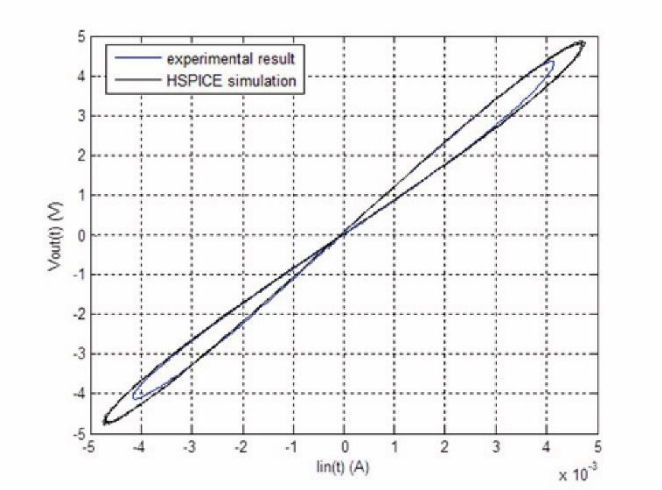
Figure 2. Obtaining the memristance from the divider configuration with the AD633JN.



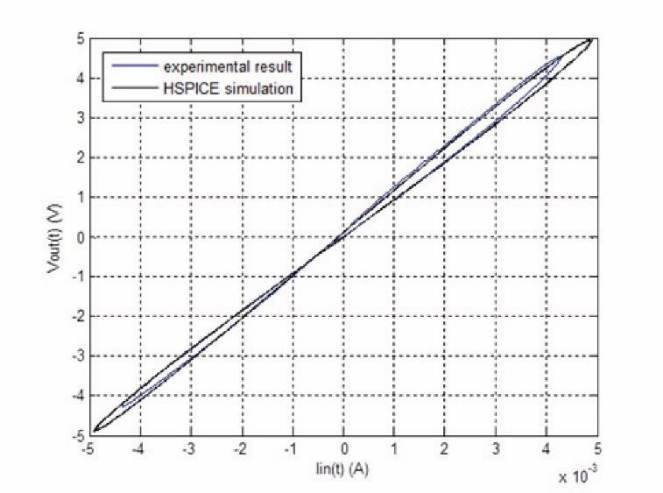
(a)



(b)



(c)



(d)

Figure 3. Experimental and HSPICE comparisons of the ffecuency-dependent pinched hysteresis loop operating at: (a) 500Hz, (b) 1 KHz, (c) 5 KHz, (d) 10 KHz.

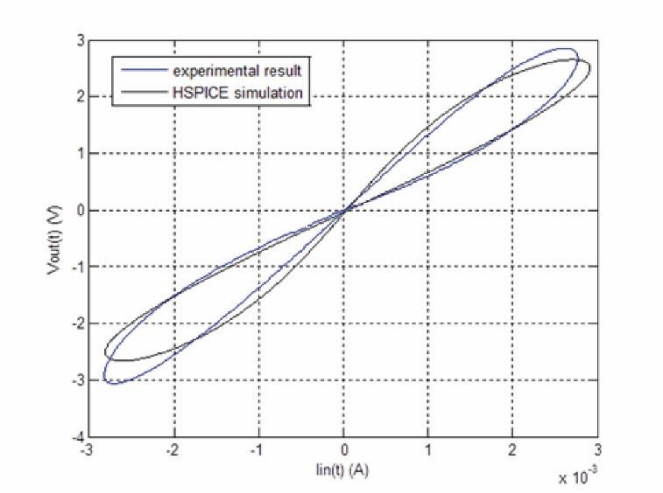
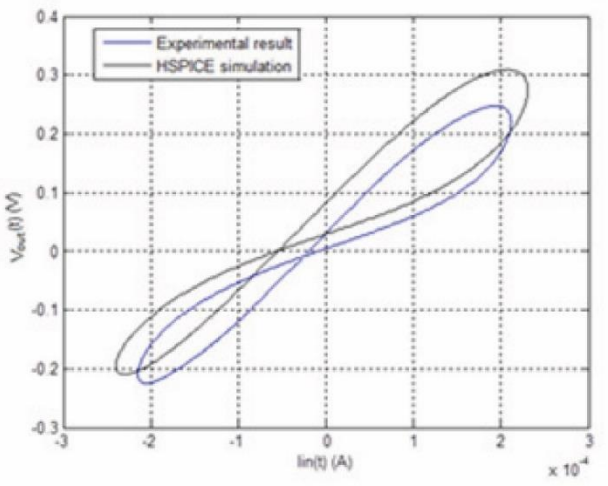
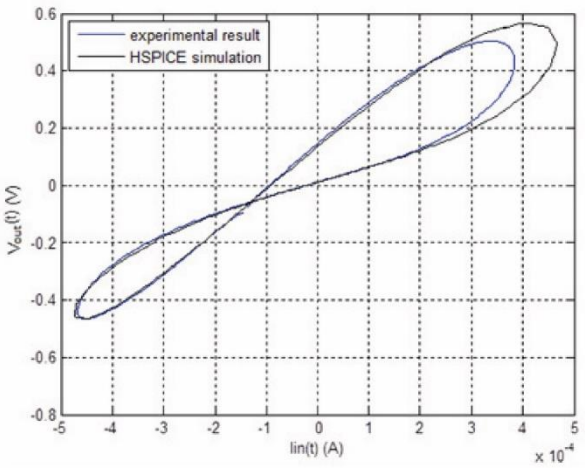


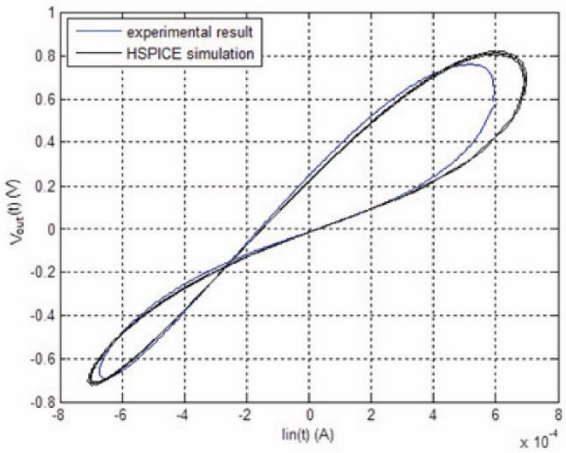
Figure 4. Experimental and HSPICE comparisons of the frequency-dependent pinched hysteresis loop operating at 1 KHz for decremental topology.



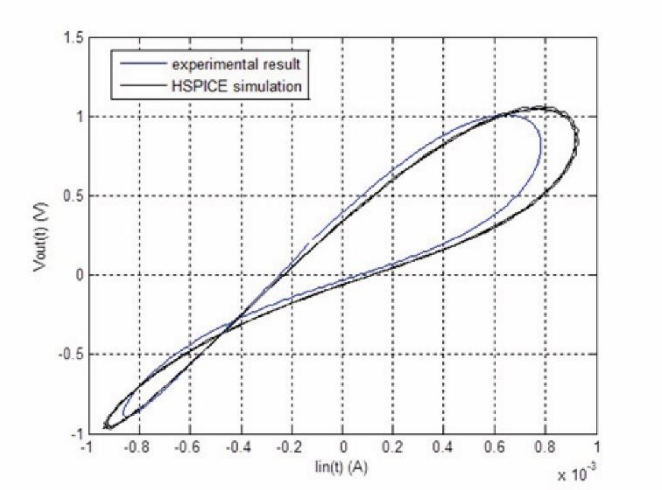
(a)



(b)



(c)



(d)

Figure 5. Comparing experimental and HSPICE results of the frequency-dependent pinched hysteresis loop operating at: (a) 50 KHz, (b) 100 KHz, (c) 150 KHz and (d) 200 KHz.

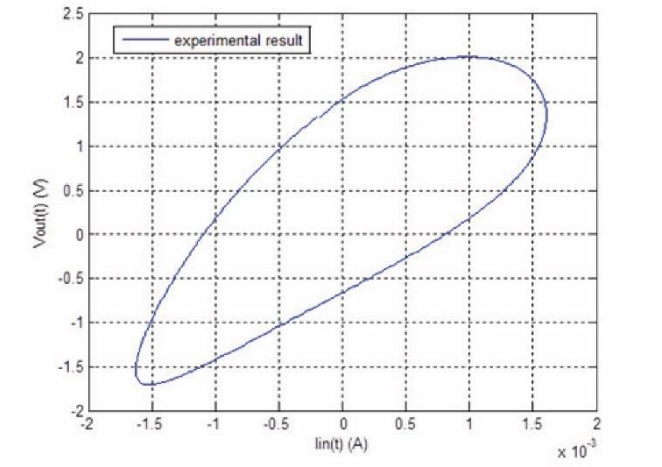


Figure 6. Experimental result of the system operating at 500 KHz.

5. Conclusions

A simple current-controlled grounded memristor emulation in incremental and decremental mode using a single commercially available active component (AD633JN) with a capacitor and a resistor has been presented. The proposed circuit also includes, through an additional divider configuration, the possibility of generating the value of the memristance. An advantage with respect to other configurations reported in the literature is that it is relatively easy to determine the magnitude of the input current at a certain frequency, avoiding reaching the maximum rating voltages of the multiplier. The corresponding output voltage

would make its use possible in applications of the memristor in voltage mode such as: Analog voltage memory with applications in arithmetic operations and filters. As for the pinched hysteresis loop, we could see that at high frequencies it loses symmetry due, among other things, to the phase shift involving the multiplication of sinusoidal functions, a shift of the loop with respect to the origin can also be observed due to the above and also to the parasitic resistances of the multiplier that give rise to the offset, which according to the manufacturer is 50 mV. As future work, it is proposed to test the behavior of the system with a multiplier with greater bandwidth. Experimental results using AD633JN multiplier device were gathered, showing good agreement with HSPICE simulations. It was not possible to obtain experimental results of the measurement of the memristance in the presence of a train of pulses because when performing divisions by zero significant errors were generated, however, the simulation give an idea of how the memristance would behave in this case.

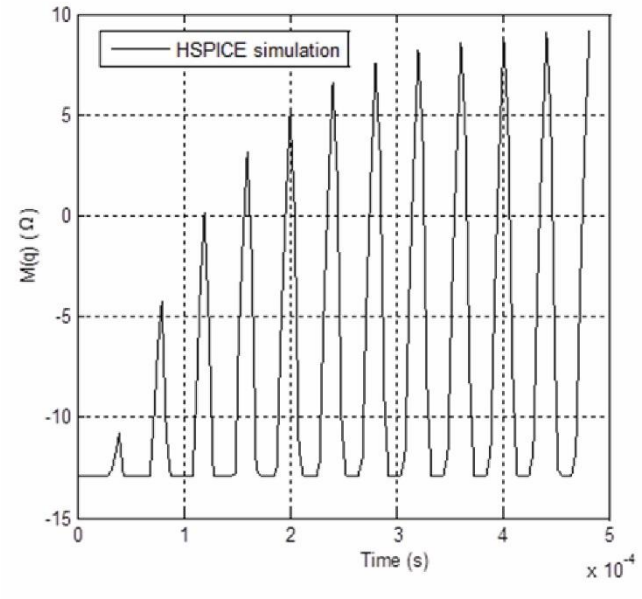


Figure 7. Simulation results of the memristance change.

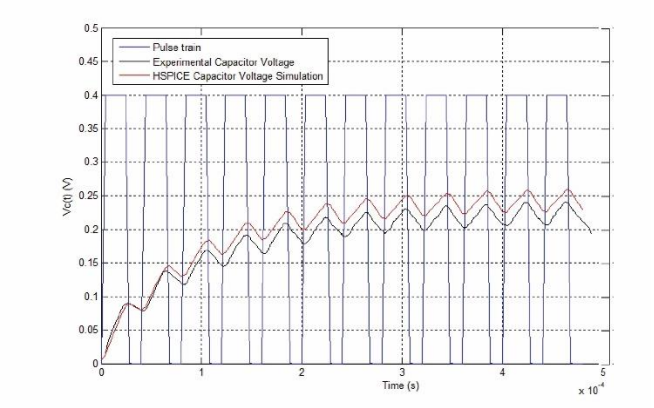


Figure 8. Simulated and experimental capacitor voltage results.

Conflict of interest

The authors have no conflict of interest to declare.

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