A PURE NODAL-ANALYSIS METHOD SUITABLE FOR ANALOG CIRCUITS USING NULLORS

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ABSTRACT

A novel technique suitable for computer-aided analysis of analog integrated circuits (ICs) is introduced. This technique uses the features of both nodal-analysis (NA) and symbolic analysis, at nullor level. First, the nullor is used to model the ideal behavior of several analog devices, namely: transistors, opamps, OTAs, and current conveyors. From this modeling approach, it is shown how to transform circuits working in voltage-mode to current-mode and vice-versa. Second, it is demonstrated that using nullors, all non-NA-compatible elements can be transformed into NA-compatible ones, this results in a computationally-improved pure-NA method. Third, the computation of fully-symbolic expressions using $MAPLEV^{TM}$, is described. It is demonstrated that a symbolic expression gives more insight in the behavior and performance of the circuit. Finally, several examples demonstrate the suitability and appropriateness of the proposed method to be used in education.

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KEYWORDS: CAD Tools, Circuit Theory, Nullors, Analog Modeling, Symbolic Analysis, Nodal Analysis.

1. INTRODUCTION

Speaking in computational lenguage the circuit is a mathema-tical object subject to computer analysis so that the most common task associated with circuit analysis is computing the mathematical representation for the circuit elements [1-2]. Mathematical analysis results in equations relating circuit performance to component values in which the best mathematical approach (circuit modeling) is usually a simplified theoretical analysis to give insight and estimates of component values [3-5]. In doing circuit analysis, it is well-known that by using symbolic analysis techniques [6-8], the designer can get a better insight in the behavior and performance of the circuit rather than by using numerical analysis like SPICE computations.

The main task of circuit analysis is to compute the values of voltages and currents, which are considered to be the responses to the given input signal excitations. However, traditional circuit analysis schemes such as the *Tableau* and Modified Nodal Analysis (MNA) methods have several computational disadvantages: they result in huge matrices even for small-sized circuits, and the main one is that they result in cumbersome computer-manipulations for non-NA-compatible circuit-elements [3-9]. That way, in order to avoid that computational-disadvantages, a pure nodal-analysis (PNA) method is introduced herein.

The proposed PNA method transforms all non-NA-compatible elements into NA-compatible ones by using nullors. Furthermore, by using the nullor properties an improved Compacted-PNA method is obtained. Additionally, by using the nullor concept, it is shown how to transform circuits working in voltage-mode to current-mode and vice-versa [8-10].

The main goal of this paper is focused on computing fully-symbolic transfer functions (TFs), i.e. H(s), of nullor circuits from the proposed PNA representation in which the output and input electrical variables can be freely chosen. Notwithstanding, the proposed method has been implemented in MAPLEV^{TM} [13]. On the other hand, an IC designer usually wants to know how the circuit performance is affected by changes in one or more parameter values. The effects of parameter changes on the circuit performance can be predicted by applying a sensitivity analysis [11]. Using the proposed PNA method, we can easily compute the sensitivity of H(s) with respect to the circuit parameter *x* in a post-processing step. Also, for rational transmittances, Bode plots become convenient for computing the frequency response of linear or linearized circuits [12]. Bode plots can be easily computed in a post-processing step by converting a fully-symbolic expression into a rational one [3-9].

2. ANALOG MODELING USING NULLORS

In 1954 Tellegen introduced the concept of "ideal amplifier", and indirectly the "nullor" concept [14]. The nullor has been used as a general building block for the implementation of linear and nonlinear analog systems [15]. The monolithic integration of this element made in [10], demonstrate its suitability to be considered as a universal active device (UAD). In this way, by resorting to the nullor concept we introduce a unified modeling approach that can be applied to the most commonly used linear or linearized circuits. It is worth to mention that the main objective of the analog modeling approach, using nullors, is related to transform all non-NA-compatible elements into NA-compatible ones, in order to provide a CAD-tool suitable for achieving the symbolic analysis of analog ICs by applying the proposed PNA method.

2.1 The mullor

This UAD has two-ports with four associated electrical variables having the following characteristics:
$\boldsymbol{V}_1, \boldsymbol{I}_1$ at its input port assume the condition that $\boldsymbol{V}_1 = 0, \boldsymbol{I}_1 = 0$. $\boldsymbol{V}_1, \boldsymbol{I}_1$ are associated to the element called *nullator*.
$\boldsymbol{V}_2, \boldsymbol{I}_2$ at its output port have arbitrary values. $\boldsymbol{V}_2, \boldsymbol{I}_2$ are associated to the element called *norator*.

The nullor is composed by a nullator-norator pair, as shown in Fig. 1; where both components have undefined impedances. As it occurs with the ideal opamp, the transfer properties of the nullor only become well defined if an external network provides for feedback from the output to the input port [9]. Depending on the kind of connection of the nullor with other passive elements, namely: resistors, capacitors and inductors; we can get several circuit implementations, as shown along the following subsections.

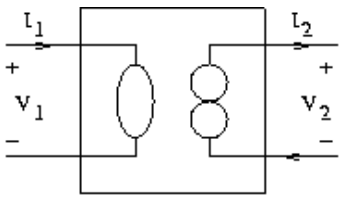

Figure 1. The nullor

2.2 Modeling an independent voltage source

An independent voltage source is a non-NA-compatible element. Using one nullor, as shown in Fig. 2, an independent voltage source is transformed into a current source, which then becomes NA-compatible.

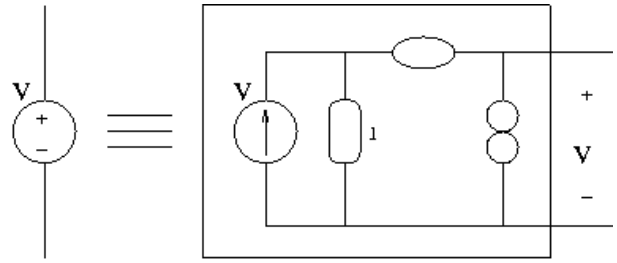

Figure 2. Transforming a voltage into a current source

2.3 Modeling a generic transistor

If the bottom terminals of the nullor are connected together but not necessarily grounded, we get a device simulating the behavior of an ideal transistor either BJT or MOSFET [5], as shown in Fig. 3.

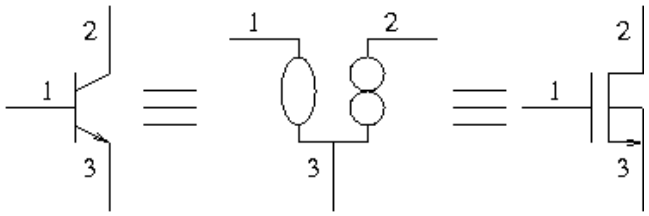

Figure 3. Modeling a generic transistor

2.4 Modeling the voltage and current followers

Depending on the connection of the nullor as a two-port element, we can get either a voltage or current follower, as shown in Fig. 4.

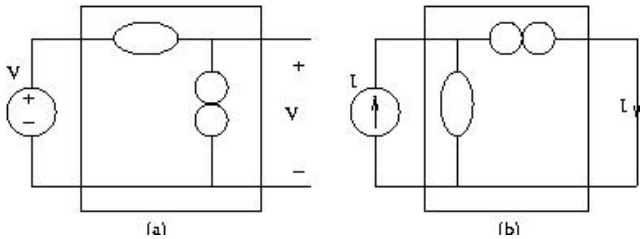

Figure 4. Modeling the voltage and current followers

2.5 Modeling analog building blocks: opamp, OTA and CCII-

Since the nullor is suitable for macro-modeling several circuits, we can model the ideal behavior of some analog building blocks, namely: the opamp, OTA and CCII-, as shown in Fig. 5. The associated mathematical port-relationships defining their ideal behavior are given as follows [9]:
Opamp: At its input port, V=I=0. At its output port V=I=undefined.
OTA: At its input port, I=0. At its output port $\boldsymbol{I_o = gV_{in}}$.
CCII-: At its input port, $\boldsymbol{I_y = 0, V_y = V_x}$. At its output port $\boldsymbol{I_z = I_x}$.

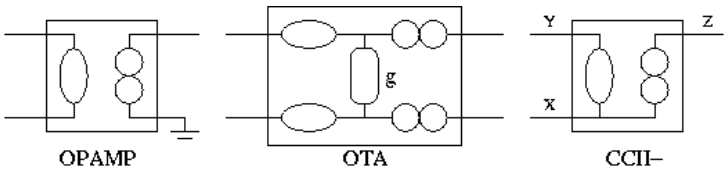

Figure 5 Modeling analog building blocks

2.6 Modeling the four controlled sources: A unified approach

Although many implementations may exist for the four controlled sources, a unified modeling approach for them using a symmetrical cell, i.e. the OTA, is shown in Fig. 6. Later on, the computational convenience of this is demonstrated.

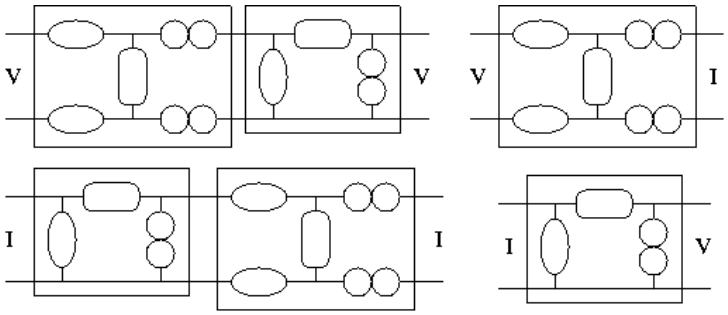

Figure 6. Modeling the four controlled sources

2.7 Transforming voltage- to current-mode circuits and vice versa

By applying the adjoint-network properties [4], it is possible to transform a nullor-based circuit working in voltage-mode into an equivalent one working in current-mode and vice-versa. The transformation is computed by applying the following four rules:

1) Set the nullator and norator references.
2) Interchange nullators by norators and vice-versa, but keeping the associated pairs, i.e. the nullors.
3) At the input port, the voltage/current source is short/open circuited. This port becomes the output port where the current/voltage has to be measured.
4) At the output port, if the load is driven by a voltage/current signal, then connect a current/voltage source. Now it becomes the input port where the current/voltage signal is supplied.

An illustrative example of this transformation-process is given in section 5.5.

3. PURE NODAL ANALYSIS

When linear circuits are modeled using nullors, the resulting network will contain only: resistors, capacitors, nullors, and independent current sources. This set of circuit elements simplifies the algorithms for computing the ac circuit analysis, as it is shown later in section 4. An important thing is that we are avoiding the computation of the stamps associated to every non-NA-compatible element (which may be very time-consuming), i.e. we are saving CPU time. Notwithstanding, the handling of the database representing the interconnection-pattern of the network becomes to be improved.

The PNA representation is focused on computing equation (1), where **i** represents the vector of independent current sources, $\boldsymbol{Y}_{PNA}$ represents the nodal admittance-matrix and **v** represents the node voltage-variables vector [3-5].

$$\boldsymbol{i} = \boldsymbol{Y}_{\boldsymbol{PNA}}\boldsymbol{v} \tag{1}$$

It clearly results that the computational effort for computing the matrix $\boldsymbol{Y}_{\boldsymbol{PNA}}$ is simpler and easier than computing the matrix MNA or the *Tableau* [3-8]. Additionally, the solution of equation (1) is simpler and easier to compute if we resort with the properties of the nullor. These properties are directly related with the handling of the rows and columns of the matrix $\boldsymbol{Y}_{\boldsymbol{PNA}}$, so that its order is reduced in one by each nullor. This reduction-process leads us to introduce a Compacted PNA method.

4. COMPACTED PNA METHOD

In equation (1), the order of the matrix $\boldsymbol{Y}_{\boldsymbol{PNA}}$ is reduced in one by each nullor by applying the following four rules [9]:

1) Add the columns associated to a floating nullator because the voltage across it is zero, i.e. both associated nodes have virtually the same potential, as shown in Fig. 7a.
2) Add the rows associated to a floating norator because the current through it is the same, as shown in Fig. 7b.
3) Delete the column associated to a grounded nullator because both nodes become virtually connected to ground, as shown in Fig. 7c.
4) Delete the row associated to a grounded norator because both nodes become virtually connected to ground, as shown in Fig. 7d.

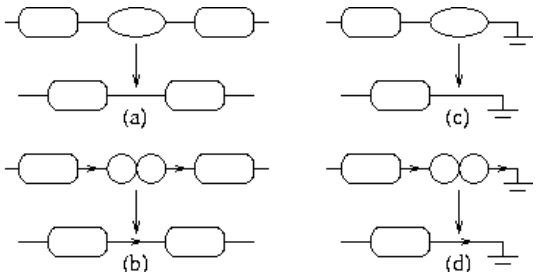

Figure 7. Rules for computing $\boldsymbol{Y}_{\boldsymbol{CPNA}}$

After applying these rules to equation (1), it results in a Compacted PNA representation given by equation (2), where the matrix $\boldsymbol{Y}_{\boldsymbol{CPNA}}$ has an order equal to the order of the original $\boldsymbol{Y}_{\boldsymbol{PNA}}$ minus the number of nullors.

$$\boldsymbol{i} = \boldsymbol{Y}_{\boldsymbol{CPNA}}\boldsymbol{v} \tag{2}$$

From this equation, one can easily compute the TF as a fully symbolic expression denoted by H(s). It is worth to mention that the computation of TFs using the proposed CPNA method is quite simpler and easier than using traditional methods based on Signal Flow Graph, Mason's Rule, and so on [3-5].

5. EXAMPLES

In order to demonstrate the suitability and appropriateness of the proposed method, we have selected several illustrative examples including the opamp, MOSFETs, the CCII-, and the OTA circuit elements.

5.1 The inverting voltage amplifier

The well-known opamp-based inverting amplifier is shown in Fig. 8. As we know, the TF of this circuit is given by equation (3).

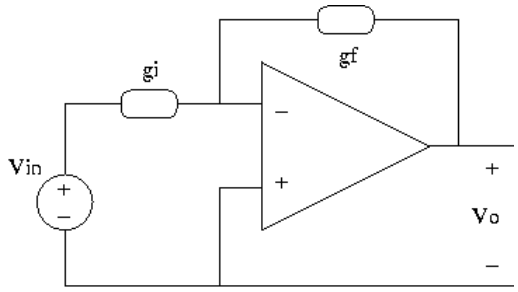

Figure 8. The inverting voltage amplifier

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i} \tag{3}$$

If we replace the voltage source and the opamp, which are non-NA-compatible elements, by its nullor-equivalent, we get the nullor circuit shown in Fig. 9, where all the elements become NA-compatibles. The computation of equation (1) is given as

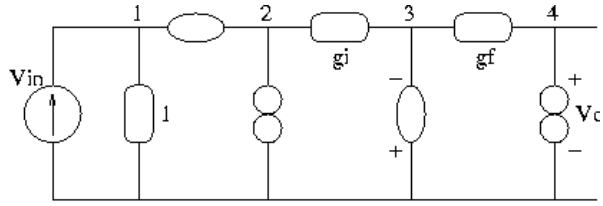

Figure 9. Nullor-circuit equivalent of figure 8

$$\begin{bmatrix} V_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & g_i & -g_i & 0 \\ 0 & -g_i & g_i + g_f & -g_f \\ 0 & 0 & -g_f & g_f \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{4}$$

After applying the rules given in section 4, we obtain the CPNA representation having an order equal to 2 (there are 2 nullors).

$$\begin{bmatrix} V_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -g_i & -g_f \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_4 \end{bmatrix} \tag{5}$$

Note that nodes 1 and 2 are virtually having the same potential, and node 3 is virtually connected to ground!. Finally, after solving for node 4 we obtain

$$v_4 = (g_i V_{in}) / (-g_f) \tag{6}$$

In terms of resistances, equation (6) happens to be of the form of equation (4), Q.E.D.

5.2 A CMOS OTA design

In Fig. 10 it is shown an OTA design providing a symmetric compensation technique that improves its

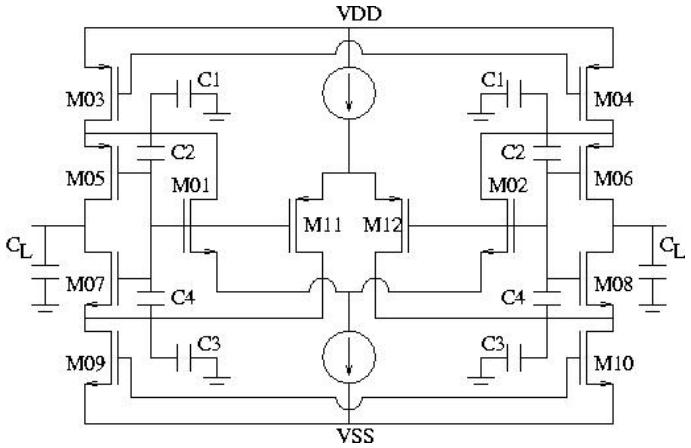

Figure 10. Symmetrically compensated fully differential folded-cascode OTA

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{i1} \\ V_{i2} \end{bmatrix} = \begin{bmatrix} g_x & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ g_3 & g_5 + s(C_1 + C_2) & 0 & 0 & g_1 - g_5 - sC_2 & 0 & 0 & 0 & -g_1 & 0 & 0 & 0 \\ g_4 & 0 & g_6 + s(C_1 + C_2) & 0 & 0 & g_2 - g_6 - sC_2 & 0 & 0 & -g_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_{11} + g_{12} & -g_{11} & -g_{12} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -g_5 & 0 & 0 & g_5 + g_7 & 0 & sC_L & 0 & 0 & -g_7 & 0 & 0 \\ 0 & 0 & -g_6 & 0 & 0 & g_6 + g_8 & 0 & sC_L & 0 & 0 & -g_8 & 0 \\ 0 & 0 & 0 & -g_{11} & g_{11} - g_7 - sC_4 & 0 & 0 & 0 & 0 & g_7 + s(C_3 + C_4) & 0 & g_9 \\ 0 & 0 & 0 & -g_{12} & 0 & g_{12} - g_8 - sC_4 & 0 & 0 & 0 & 0 & g_8 + s(C_3 + C_4) & g_{10} \\ 0 & 0 & 0 & 0 & -g_1 & -g_2 & 0 & 0 & g_1 + g_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & g_4 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_4 \\ v_5 \\ v_6 \\ v_{7,9,11,15,18,25} \\ v_{8,10,12,16,19,26} \\ v_{13} \\ v_{14} \\ v_{17} \\ v_{20} \\ v_{21} \\ v_{22,23,24} \end{bmatrix}$$

After computing the voltage TF, for $g_{m1} = g_{m11}$, $g_5 = g_7, g_3 = g_9, C_1 = C_3$ and $C_2 = C_4$ we obtain the following equation given in [16]:

$$\frac{V_o}{V_{in}} = -\frac{g_{m1}}{g_o} \frac{\left(1 + s\frac{C_1}{g_{m1}}\right)}{\left(1 + s\frac{C_L}{2g_o}\right)\left(1 + s\frac{C_1 + C_2}{g_{m5}}\right)} \tag{7}$$

where the output conductance becomes

$$g_o = \frac{g_7(g_{m1} + g_9)}{g_7} \tag{8}$$

5.3 A CCII- based GIC implementation

In this example, is exploited the potential of the nullor as a fully floating device [10]. In Fig. 12 it is phase response, as demonstrated in [16]. The computation of the voltage TF is done from the gates of transistors M01, M02, M11, M12, where the input is connected, to the drains of transistors M05, M06, M07, M08, where the output is measured. The nullor circuit equivalent of the symmetrically compensated fully differential folded-cascode OTA is shown in Fig. 11. In this Figure, it is omitted the inclusion of the nullor-equivalent for the voltage source, in order to have a better sight. Also, there are shown only the nodes located at the input and output ports. Note that each MOSFET has been replaced by its nullor-equivalent where their trans-conductance is modeled by a conductance connected at their source.

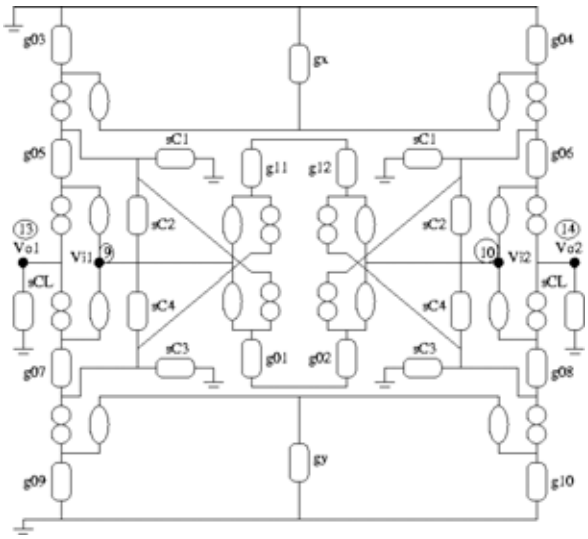

Figure 11. Nullor-circuit equivalent of figure 10

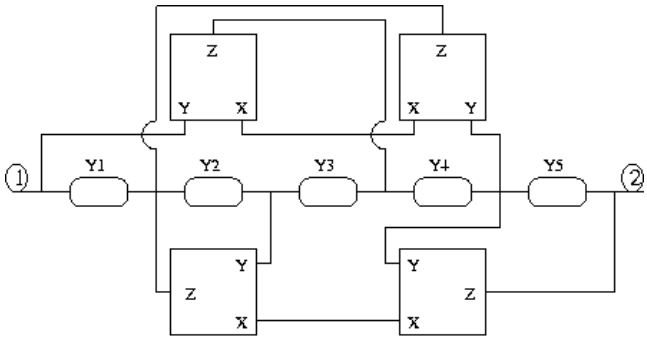

Figure 12. Floating structure for GIC implementation using CCII-s

The computation of equation (1) has a matrix $\boldsymbol{Y}_{PNA}$ having an order 26×26. However, since the circuit has 14 nullors, the computation of equation (2) has a matrix $\boldsymbol{Y}_{CPNA}$ having an order 12×12, as shown in the formulation given below:

Shown a CCII- based GIC that allows the simulation of several different either floating or grounded impedances. The nullor equivalent of this circuit is given in Fig. 13. In order to compute a TF having a transadmittance nature, i.e. I/V, a current source is connected across the floating nodes. Furthermore, the CPNA formulation requires to have a datum node, which for simplicity we select node 6. Finally, the computation of equation (2) is given in equation (9).

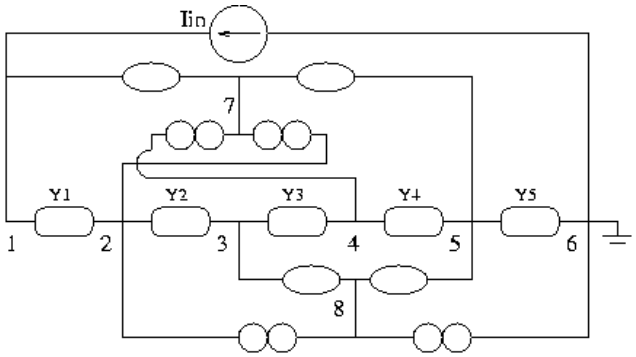

Figure 13. Nullor-circuit equivalent of figure 12

$$\begin{bmatrix} \boldsymbol{I_{in}} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_1} & -\boldsymbol{Y_1} & 0 \\ \boldsymbol{Y_2}+\boldsymbol{Y_3} & -\boldsymbol{Y_2} & -\boldsymbol{Y_3} \\ \boldsymbol{Y_4}+\boldsymbol{Y_5} & 0 & -\boldsymbol{Y_4} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{1,3,5,7,8} \\ \boldsymbol{v}_2 \\ \boldsymbol{v}_4 \end{bmatrix} \tag{9}$$

Computing for the voltage at node 1 we obtain

$$\boldsymbol{v}_1 = \frac{\boldsymbol{I_{in}}\boldsymbol{Y_2}\boldsymbol{Y_4}}{\boldsymbol{Y_1}\boldsymbol{Y_2}\boldsymbol{Y_4} + \boldsymbol{Y_1}\left[-\boldsymbol{Y_4}\left(\boldsymbol{Y_2}+\boldsymbol{Y_3}\right)+\boldsymbol{Y_3}\left(\boldsymbol{Y_4}+\boldsymbol{Y_5}\right)\right]} \tag{10}$$

Finally, the transadmittance equation is given as

$$\frac{\boldsymbol{I_{in}}}{\boldsymbol{v}_1} = \boldsymbol{Y_{in}} = \boldsymbol{Y}_{1-6} = \frac{\boldsymbol{Y_1}\boldsymbol{Y_3}\boldsymbol{Y_5}}{\boldsymbol{Y_2}\boldsymbol{Y_4}} \tag{11}$$

5.4 A lossy $\boldsymbol{G_m}$-C integrator

The circuit shown in Fig. 14, behaves as a lossy integrator, it is implemented by using two OTAs and one capacitor. The nullor equivalent of this circuit is shown in Fig. 15. The computation of the voltage TF is done as follows: as it can be seen, the circuit has 7 nodes, so that the matrix $\boldsymbol{Y_{PNA}}$ has an order 7×7. However, since the circuit has 5 nullors, then

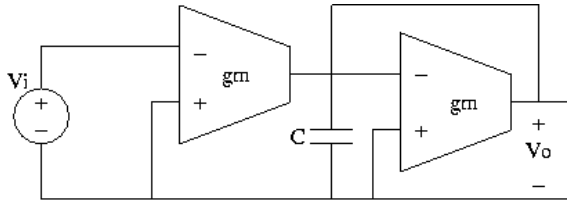

Figure 14. A lossy Gm-C integrator

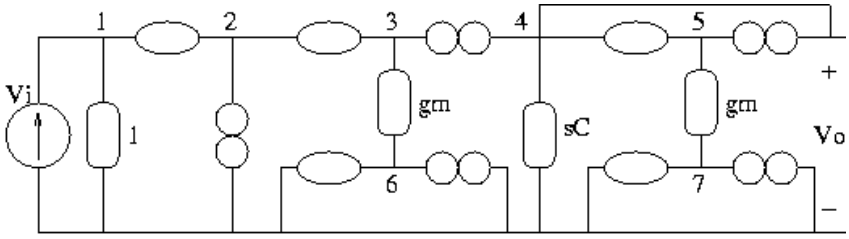

Figure 15. Nullor-circuit equivalent of figure 14

the matrix $\boldsymbol{Y_{CPNA}}$ will have an order 2×2!!!, as shown below:

$$\begin{bmatrix} \boldsymbol{V_{in}} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \boldsymbol{g_m} & \boldsymbol{sC}+\boldsymbol{g_m} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{1,2,3} \\ \boldsymbol{v}_{4,5} \end{bmatrix} \tag{12}$$

By computing the voltage at node 4, we obtain

$$\boldsymbol{v}_4 = \frac{\boldsymbol{V_{in}}\boldsymbol{g_m}}{\boldsymbol{sC}+\boldsymbol{g_m}} \tag{13}$$

Finally, the voltage TF of the lossy Gm-C integrator becomes

$$\frac{V_o}{V_{in}} = \frac{1}{1 + s\frac{C}{g_m}} \tag{14}$$

5.5 Transforming voltage- to current-mode circuits

In order to transform a circuit working in voltage-mode, e.g. the one shown in Fig. 14, to the one working in current-mode: the resulting nullor equivalent must include the independent input-voltage source, as shown in Fig. 16a. From this figure, we can apply the transformation rules given in section 2.7. By applying rule 2, the interchange of nullators by norators and vice-versa, but keeping intact the external circuitry, is shown in Fig. 16b. The application of rules 3 and 4 is shown in Fig. 16c.

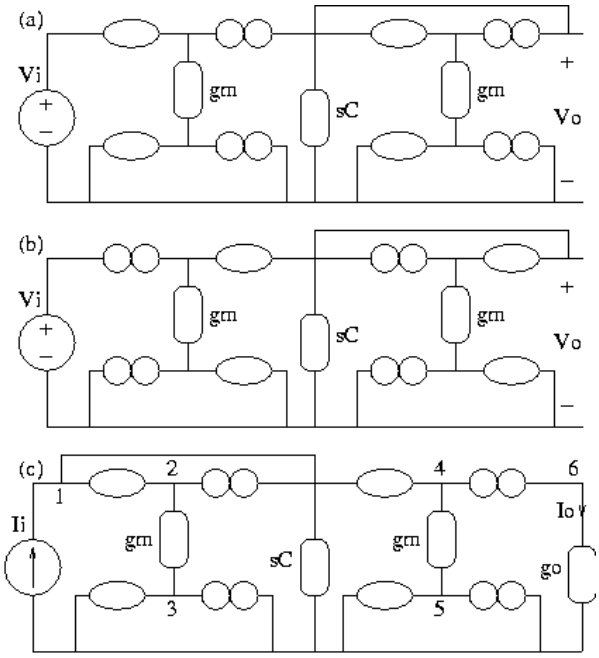

Figure 16. Transforming a circuit working in voltage- to current- mode. Applying (a) rule 1, (b) rule 2 and (c) rules 3-4 of section 2.7

If we apply the proposed CPNA method for computing the current TF of the nullor circuit shown in Fig. 16c, we should insert a load-conductance where the output current must be measured. Afterwards, the output current is obtained by computing the voltage across this conductance and through computing the expression I=gV. Therefore, equation (2) is computed as

$$\begin{bmatrix} I_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} sC + g_m & 0 \\ g_m & g_o \end{bmatrix} \begin{bmatrix} v_{1,2,4} \\ v_6 \end{bmatrix} \tag{15}$$

The voltage at the output port becomes

$$v_6 = \frac{I_{in} g_m}{g_o (sC + g_m)} \tag{16}$$

Finally, by computing the expression $I_o = g_o v_6$, we obtain the current TF expressed as

$$\frac{I_o}{I_{in}} = \frac{1}{1 + s\frac{C}{g_m}} \tag{17}$$

If we replace each pair of nullors connected across a transconductance by an OTA, we obtain a lossy Gm-C integrator working in current-mode, as shown in Fig. 17.

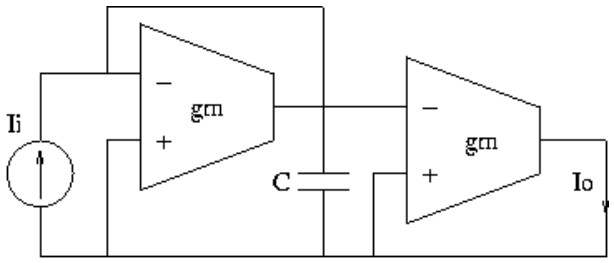

Figure 17. A current-mode lossy Gm-C integrator

6. CONCLUSIONS

A pure nodal-analysis method suitable for analog circuits using nullors has been described. It was demonstrated that this technique avoids the manipulation of large matrices such as in the MNA and Tableau methods. Furthermore, this technique avoids the use of *stamps* through transforming all non-NA-compatible elements into NA-compatible ones by using nullors. Most important is the fact that using the nullor properties, a Compacted PNA formulation is obtained by handling the columns and rows of the matrix Y_{PNA}. That way, the order of the matrix is reduced in one by each nullor. It was also shown that the matrix Y_{CPNA} is easier to set up than either, the matrix Y_{MNA} or the *Tableau*, leading to an improvement on the CPU time. The proposed CPNA method uses the features of symbolic analysis.

The examples shown in section 5 demonstrate the suitability and appropriateness of this technique to be used as an analytical method. Additionally, as one sees, this technique deals with a more general class of analog circuits, covering the gap between Hardware Description Languages and circuit-oriented simulators. Another important thing is that using nullors, circuits working in voltage-mode can be transformed to work in current-mode and vice-versa.

Since this work was based on ideal concepts, the proposed PNA method must be used only if low accuracy is required, otherwise, a more accurate modeling process should be developed precise.

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