LOW NOISE LOW POWER READOUT CIRCUIT FOR SOFT X RAY DETECTION

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ABSTRACT

A new low power CMOS ASIC for the detection of X-rays was optimized for low power and low noise. Theoretical calculations and optimizations are presented and compared with experimental results. Noise as low as $120+25 \cdot C_{in}$ [pF] ENC rms was obtained including a silicon detector of 1.3 pF and 0.3nA of leakage. The power consumption is less than 100 W. Other circuit parameters are also shown.

KEYWORDS: Charge sensitive amplifiers, Equivalent noise charge, Sharper.

1. INTRODUCTION

During the last years, an important effort has been dedicated to the development of electronics circuits for nuclear radiation measurements using crystalline and amorphous silicon diodes detectors. Recently we reported [1] a full custom integrated circuit designed for X-ray photon detection in a new system approach to digital radiography. For pixel array architectures, a big amount of pixels is needed to obtain high resolution and thus low power consumption and small area per channel are required in the readout circuits. Detection of soft X-ray used in medical applications also requires high gain preamplifiers and very low overall noise in the circuit. In this paper we present calculations and experimental results obtained for low noise optimization, while maintaining low power consumption and other required parameters.

2. READOUT CIRCUIT CHARACTERISTICS

The front end of the readout circuit consists of a Charge Sensitive Amplifier (CSA), designed to integrate the charge collected at the detector during a period of time much bigger than its collection time in order to create a voltage pulse at the output of the circuit. CSA are low bad pass filters with an integration time mainly dependent on the output impedance, peak voltage and feedback capacitor. Their noise is mainly due to the high transconductance input MOS transistor. To cut this unnecessary noise a narrow band filter called Shaper must be included and its parameters optimized to achieve required signal to noise ratio. JFTET transistors have less noise than MOS, but are difficult to implement using standard CMOS technology employed in our circuit.

Fig. 1 shows the first two blocks of the ASIC corresponding to the CSA and SHP, designed to obtain a maximum output voltage swing of 3V, a shaping time less than 5 μs for a capacitive load of 20 pF, a power consumption less than 100 μW and a single voltage supply of 5V, so it can be used in portable systems, space and big matrix detectors. The calculated gain was 3446 mV/fC, to allow detection of charges above 400 electrons, if noise is maintained below 200 electrons. The detector used in [1] had a capacitance of $C_d = 1.3\ pF$ and diode leakage of $Is = 0.35\ nA$. Fig. 2 shows the schematics of the detector diode with an AC coupling to the readout circuit.

3. NOISE OPTIMIZATION

Noise was theoretically minimized optimizing the detector bias resistor R_{BIAS}, the input transistor transconductance g_{m1}, and the shaping time of the filter τ. The noise in the circuit, expressed by the Equivalent Noise Charge (ENC) at the input, was calculated through equations [2,3]:

$$ENC_d = \sqrt{\left(2qI_L + \frac{4kT}{R_{bias}}\right) * \tau * \frac{(1.57 * 7.39)}{q^2 4\pi}} \qquad (1)$$

$$ENC_{th} = \sqrt{\frac{8}{3} kT \frac{1}{g_m} \frac{C_t^{\ 2}}{q^2 4\pi\tau} (1.57 * 7.39)} \qquad (2)$$

$$ENC_f = \sqrt{\frac{K_f}{C_{ox}^{\ 2} WL} \frac{C_t^{\ 2}}{q^2 2} (1.57)} \qquad (3)$$

where detailed description of the parameters and their values are shown in Table I.

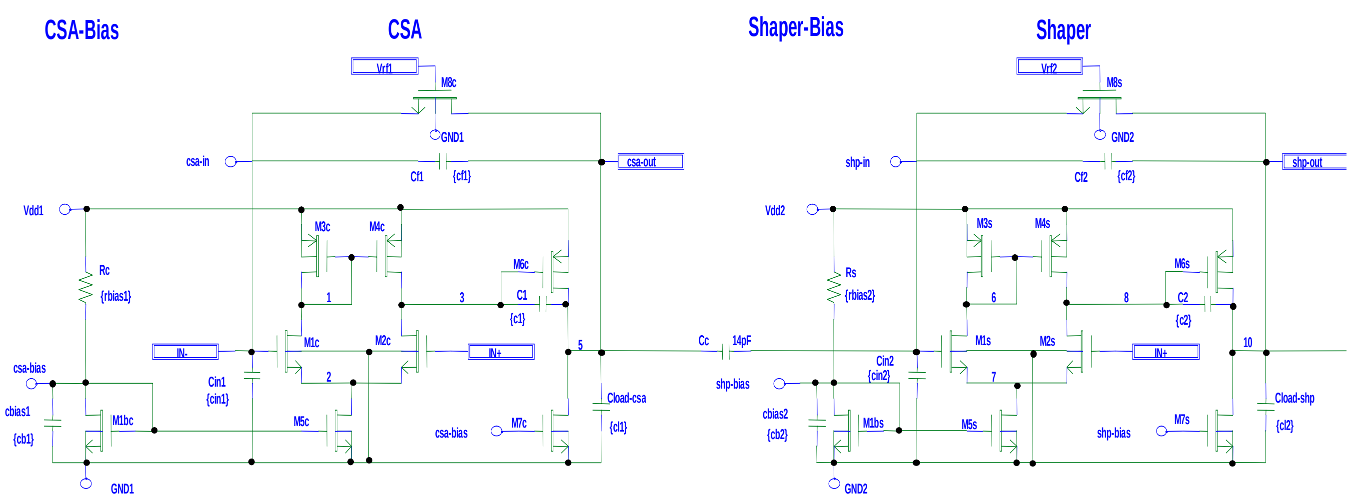

Figure 1. Electronic readout circuit of the channel including the integrator CSA and Shaper.

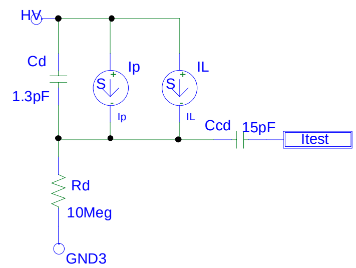

Figure 2. Model of a detector diode connected in AC.

Total noise is calculated by:

$$ENC_{tot}^{2} = ENC_{th}^{2} + ENC_{f}^{2} + ENC_{d}^{2} \tag{4}$$

Optimized shaping time was calculated using the condition:

$$\frac{dENC_{tot}}{d\tau} = 0\,, \tag{5}$$

obtaining the value:

$$\tau \cong C_t \sqrt{\frac{8kT/3g_m}{2qI_L}} \tag{6}$$

The dependence of ENC_{tot} on each of the parameters is calculated using a program written in “Mathematica“ and is shown in Fig. 3. Table I indicates the optimized and used parameters in the circuit design and optimization.

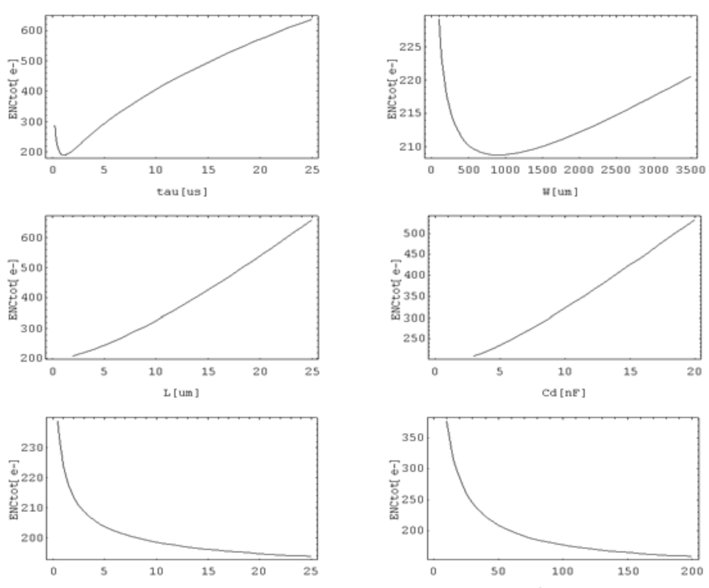

Figure 3. Dependence of ENC_{total} vs. all other parameters, using values reported in Table 1, for T=300 °C.

Table I. Optimized and other circuit parameters for ORBIT 2 μm, N well process.

Parameter (description)	Symbol	Value	Unit
Channel width of the input transistor of the CSA	W	788	μm
Length width of the input transistor of the CSA	L	2	μm
Lateral diffusion of the input transistor of the CSA	L_D	0.112	μm
Current in the input transistor of the CSA	I_{ds}	3	μA
Transconductance of the input transistor of the CSA	g_m	352.5	μA/V
Detector diode capacitance	C_d	1.3	pF
Total capacitance at the CSA input	C_t	4.16	pF
Leakage current in the detector diode	I_L	0.3864	pA
Bias resistor for the AC connection in the detector diode	R_{bias}	50	MΩ
Feedback capacitance of the CSA	C_f	30	fF
Feedback resistance of the CSA	R_f	> 100	MΩ
1/f technology process coefficient	K_f	$1x10^{-27}$	C^2/m^2
Time constant of the Shaper	τ	2.1	μs
Technology transconductance parameter	K'	52.5	$\mu A/V^2$
Integrator order	n	1	-

ENC rms noise for each of the contribution was:

ENC_{th} = 96.2311 electrons
ENC_f = 21.1393 electrons
ENC_d = 184.15 electrons
ENC_{tot} = 208.85 electrons (with detector)
ENC_{tot} = 98.5256 electrons (without detector)

4. NOISE MEASUREMENTS

We used two different methods to measure the noise. In the first method the output waveform of the Shaper is stored and analyzed using a digital oscilloscope. Fig 4a shows the pulse characteristics, while Fig. 4b shows noise at the output of the circuit without detector for an input capacitance of $C_{in} = 3pF$.

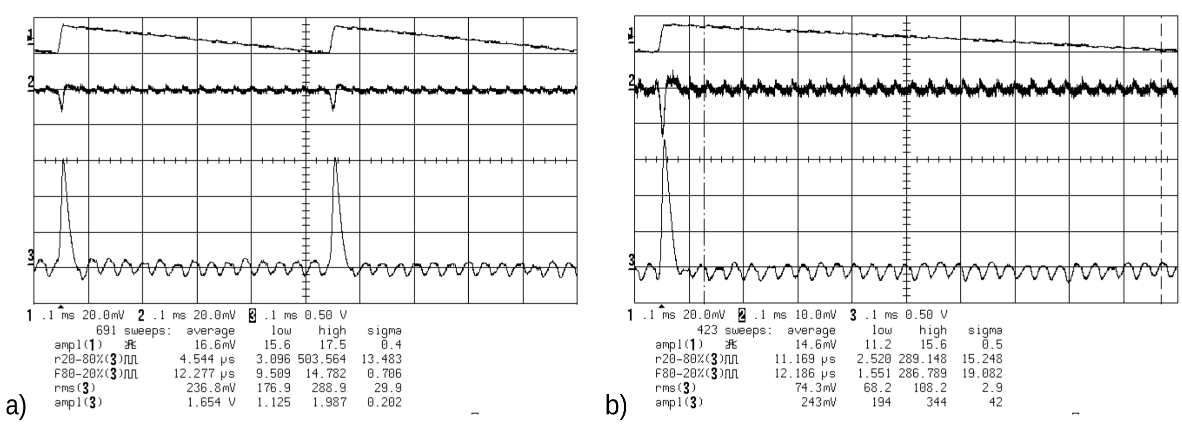

Figure 4. a) Curve (1)- CSA input signal equivalent to 3000 electrons; curve (2) - CSA output signal and curve (3)- Shaper output signal. All points in the memory are included for mathematical processing. b) Curve (1) - CSA input signal equivalent to 3000 electrons; curve (2)- CSA output signal and curve (3)- Shaper output signal. Only the points inside the window were included for mathematical processing.

ENC was calculated from *ampl(3)* in Fig.4a and *rms(3)* in Fig.4b using the following relations:

$$ENC = \frac{(ampl(1)[electrons])(rms(3))}{ampl(3)} = \frac{3000 electrons \cdot 74.3 mV}{1.654 V} = 134 electrons \qquad (7)$$

Repeating the same for different values of input capacitance, points were traced and fitted to the equation:

$$ENC_{experim}\ [electrons] = 120 + 2.5 * C_{in}\ [pF], \qquad (8)$$

The second method used was to vary the amount of injected charge by changing the peak input voltage pulse applied through a capacitance equal to the CSA feedback capacitance. The output of the Shaper was connected to a counter with a fixed threshold voltage of 4 V. The pulse generator was set in burst mode with 2000 pulses. The amount of pulses was counted for each voltage step and different input capacitance values indicated in Table 2.

The pulse amplitude vs Cin was plotted for each column in Table 2; differentiated and fitted to a gaussian function. The width of each adjusted function is a double sigma (2μ) shown in Table 3. The linear equation that better fits to all μ points can be expressed as:

$$ENC_{theor}\ [electrons] = 90 + 2.5 * C_{in}\ [pF], \qquad (9)$$

Table II. Input voltage pulses in [mV] vs. the amount of pulses counted, by the counter at the shaper output, for different input capacitance values in [pF].

Pulse [mV]	***Cin*** [pF]								
	0	3.4	6.02	9.86	17.3	26.7	39.6	47.4	55.6
6	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	2
8	0	0	0	0	1	1	4	7	33
9	0	204		69	157	186	171	157	276
	1990	2000	1999	1986	1922	1661	1199	1043	1152
	2000		2	2000		1995	1830	1774	1736
12	2000	2000	2000	2000	2000	2000	1999	1992	1977
13	2000	2000	2000	2000	2000	2000	2000	2000	2000

Table III. Width of the gaussian curve (ENC rms) for each value of input capacitance [pF].

***Cin* [pF]**	***ENC* [mV] (2σ)**	**(2σ)**	**(σ)**
0	0.81776	163.552	81.776
3.4	1.1946	238.92	119.46
6.02	1.0514	210.28	105.14
9.86	1.0222	204.44	102.22
17.3	1.2045	240.9	120.45
26.7	1.4591	291.82	145.91
39.6	1.8779	375.58	187.79
47.4	1.9731	394.62	197.31
55.6	2.1545	430.9	215.45

From both experimental methods used above to calculate the noise of the circuit we see that values are similar, that confirm the accuracy of measurements, and indicates correctness of theoretical optimizations, *ENC=98 electrons* against the experimental one *ENC=123 electrons*. The small difference can be attributed to circuit parasitic capacitances that change the filtering properties.

5. CONCLUSIONS

Theoretical calculations for noise optimization and experimental measurements of the noise in a low power, high output swing readout circuit for signal particle detection is presented, which ensure detection of as low as 400 electrons. Validity of the theoretical prediction is demonstrated using 2 methods to determine the experimental noise. The circuit presents noise as low as $ENC_{tot}=123$ *electrons* rms for $C_d=1.3$ *pF* input capacitance while keeping a power consumption lower than 100 W, and providing an output swing of 3 V which can be analyzed by laboratory equipment without other amplification stages.

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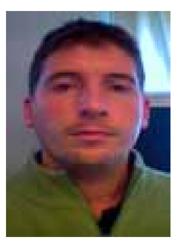

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Born in Habana, Cuba in the 1967, electro-physical engineer and master graduate from Moscow Energy Institute, Russia, in 1992. Doctorate in Sciences in the year 2000 in the IPN-CINVESTAV Mexico. He worked during 5 years in development of devices and integrated circuits for the nuclear physics, particularly the nuclear medicine and the astrophysics in the Habana Nuclear Center of Development, Cuba, and in the International Center of Physical Theoretician of Trieste, Italy. Among the works carried out there are a digital system of mammogram and a gamma rays telescope. Currently works for the DAI Telecom, Italy, in the design of new circuits integrated and teams for telecommunications, particularly, in cell phones GSM and UMTS.

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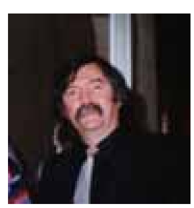

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