PERFORMANCE OF A NEW BUS ASSIGNMENT ALGORITHM FOR AN ATM SWITCH FABRIC

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ABSTRACT

This paper presents the results of the performance evaluation, through analytical and simulation models, of a High Speed Packet Switch with a New Bus Assignment Algorithm, designed and developed at the Research and Advanced Studies Center of National Polytechnic Institute in Guadalajara, México (CINVESTAV-GDL). The analytical model is tested under two different arrival processes: Binomial and Poisson distributions. The simulation model is tested with two bus assignment algorithms: Fixed Start and Rotated Start . The performance parameters considered are: Cell Loss Rate, Delay and Throughput.

KEYWORDS: ATM Switch, Bus assignment algorithm, Cell loss rate, Poison arrivals, Throughput.

1. INTRODUCTION

Since the 1980's telecommunications have experienced without precedent evolution in aspects such as: network services, traffic volume, diversity of technologies and user applications. Early, communication networks were used to carry only voice traffic. Nowadays, the networks carry multimedia traffic (voice, video and data), using digital circuit-switched and packet-switched networks [1].

Due to the evolution in this area, particularly in sophisticated networks, it arose the need for new techniques for the analysis, design and evaluation of these networks. Lately, computer simulation techniques have been gaining popularity for modeling and analysis of telecommunications networks, since they facilitate the study of complex systems and processes very difficult to analyze by traditional methods.

The modeling by analytical and simulation techniques provides a general description about the operation of complicated networks, facilitating the performance evaluation for a given traffic. The mathematical analysis consists of one or more equations that express one of the system variables in terms of fixed parameters and other variables of the same system. On the other hand, the simulation includes the development of models in software, which typically consists in writing and developing the code that represents the operation the network [2]. The simulation is normally preferred when the system is very complex and the mathematical analysis would be intensive.

Nevertheless, it is possible to obtain a more complete and detailed analysis by comparing the results of both methods [3].

Analysis and simulation techniques are used in this work to evaluate the performance of a high speed packet switch, compatible with the Asynchronous Transfer Mode standard (ATM), designed and developed in CINVESTAV-GDL.

The main objectives of this work are:

- to discuss the development of equations for calculating the performance parameters for a specific cell switch fabric, using both Binomial and Poisson arrival processes,
- to study the implementation impact of different bus assignment algorithms on a cell switch fabric, using a simulation model based on OPNET, and,
- to compare the simulation performance results with those obtained analytically.

The main contribution of this work consists in implementation of a rotational bus assignment algorithm, which increases the number of the input port that starts using the shared bus (after each cycle), thus producing an even probability of loss for all input ports. The use of a fixed cyclic assignment algorithm produces a non-uniform distribution of the traffic carried from the input ports, resulting in more losses for ports of greater index.

This paper is organized as follows: section 2 discusses briefly the characteristics of the switch operation; in section 3 performance analysis (by using Binomial and Poisson arrivals) is developed; section 4 reports the results obtained by simulation and compares them with those of the analysis, and finally section 5 presents conclusions of this work.

2. THE PACKET SWITCH

The ATM packet switch developed in CINVESTAV-GDL is composed of the following modules: *Line Interface Circuits* (LC) including their *Routing Tables* (RT) and a *Cell Switch Fabric* (SF). The LC is the interface between the selected application protocol and the cell switch fabric, and translates the packets coming from the application into self addressed 56 *bytes* long cells. The reverse process is made for data going in the opposite direction. The routing table adds the information needed to transfer the cells from the source to the destination ports, allowing the automatic routing of cells ([4]). The cell switch fabric contains 16 bidirectional ports in 4 modules. It has the responsibility of transferring packets from the input to output ports, without blocking them and with the minimum possible delay, maintaining the cell arrival order.

The switch fabric was designed as a basis for an ATM switch that supports data rates of 155.52 Mbps per port. Nevertheless, this SF uses an internal format in which the cells are 56 *bytes* long, 3 more bytes that ATM cells. These are added by the LC as a routing label. This change in the cell size, increases the data rate from 155.52 to 164.323 Mbps. The internal cell format used by the switch fabric is reported in [6].

2.1 Switch Fabric Architecture

The external common bus architecture is used in the cell switch fabric. This consists of a modular design formed by the following blocks: Input Elements (IE), Common Bus (CB), Output Elements (OE), Switch Fabric Control Block (SCB), and Test and Supervision Block (TSB). A block diagram is shown in figure 1, more details can be found in [5], and [6].

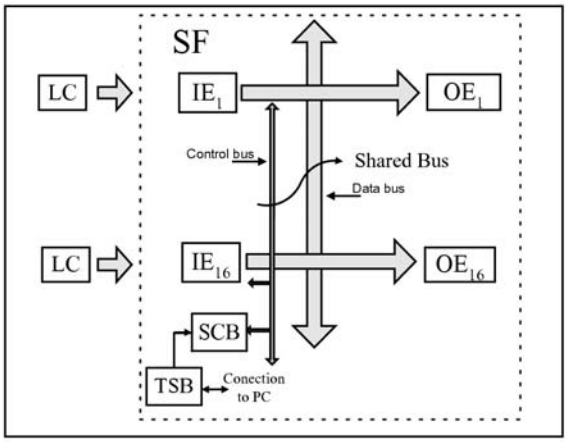

Figure 1. Switch Fabric Architecture

2.1.1Input Element

Each input port has an IE that receives cells from the LC. These cells are divided in 7 micro-cells of 64 bits in length each, and are delivered to the shared bus.

2.1.2 Common Bus (CB)

The common bus is the shared space through which the information flows from each IE to one or more OEs. To do this an interlaced micro-cell frame of same length as the cell period (bus cycle) is created. This period has duration of 2.7263 μ sec, and is called T_c .

2.1.3 Output Element (OE)

Similar to the input ports, each output port has assigned an OE, which filters the cells on the data bus and extracts the cells going to the corresponding output port. Cells are then formatted to transfer them to the LC. Each OE can receive up to 16 cells in a bus cycle (one by port) and simultaneously transmit a complete cell towards the LC.

For assembling cells, the output queue is divided in 36 consecutive locations of 56-*bytes*, so it has space for storing 16 cells from the input ports in each of two consecutive cycles, plus 4 spare locations.

2.1.4 Switch Fabric Control Block (SCB)

This block implements the bus assignment algorithm for the cell transfer and consequently, it generates the common signaling to coordinate the operation of the remaining switch blocks.

The use of a fixed cyclic assignment produces a non- uniform distribution of the traffic carried from the input ports, producing more losses in ports of greater index. Due to this disadvantage a new scheme was proposed, in this one the bus assignment sequence is rotated after each cycle, so every input port has the chance to be first in the sequence, thus producing an even probability of loss for all input ports.

2.1.5 Test and Supervision Block (TSB)

The TSB performs the self-diagnostic of the system blocks using hardware and software operations. This block also provides performance statistics of the switch fabric through a serial port for display in a terminal. For more details about the switch fabric design see [6] and [7].

3. PERFORMANCE ANALYSIS

In this section a mathematical model for the already described switch is presented. This model consists of a set of equations related to the system parameters and variables, that reflect the performance of the switch. The model is made under some assumptions that simplify the mathematical analysis. In the first case, it is based on the *M/D/1/k* queue since the cell arrivals are considered independent with Poisson distribution and the cells are served at a constant rate (deterministic time). In the second case the model corresponds to a *B/D/1/k* queue, since arrivals are considered with a binomial distribution.

Several simplifying assumptions are introduced to obtain a mathematically tractable model. The *first assumption* is that the system is in steady state. The *second one* is that the arrivals are completely random and independent. *The third assumption* is related to the arrival process: when the number of sources is infinite, the cell arrival is characterized by a Poisson process, and when a finite number of sources is assumed the arrival process is described as a Binomial distribution [8]. Both cases are analyzed separately in this work, with different models for each case.

The analysis is focused on the output stage, which consists of a FIFO queue and its corresponding server and has the characteristic to store a cell while servicing it. When a cell arrives at the destination port, it is placed in the server if it is empty, otherwise the cell is stored in the queue. Hence the system can keep up to Q = q + 1 cells during a bus cycle, where q is the queue size and the added location is due to the storage characteristic of the server. Note that, the location currently being emptied by the server, can not be used by a cell arriving to the FIFO during the same bus cycle.

Queue analysis is used here to obtain the probability that the system is found in a particular state at any time. Besides, the system is assumed to be in steady state, that is, the average number of arriving packets is equal to the average of packets leaving the switch. Under these assumptions, the state probability for a stationary system is given by:

$$P_n = [P_0 + P_1]A_n + P_2A_{n-1} + P_3A_{n-2} + \ldots + P_nA_1 + P_{n+1}A_0 \quad , \tag{1}$$

where:

A_n : probability of arrival of n cells.

P_n : probability of finding the system in state n, which means that the output queue contains n cells.

By solving equation (1) for n = 0; P_1 is obtained in terms of P_0 and the arrival probability A_0. Evaluating the same equation for n = 1, P_2 is obtained in terms of A_0 and a factor X_2 , which depends on the arrival probabilities A_0 and A_1. Using this method iteratively, P_n can be obtained in terms of P_0 and the X_i factors from i = 2 to n. X_n are dependent on the arrival probability as in equation (2):

$$X_n = X_{n-1}\left(\frac{1-A_1}{A_0}\right) - \sum_{k=1}^{n-2} X_k\left(\frac{A_{n-k}}{A_0}\right) - \frac{A_{n-1}}{A_0} \tag{2}$$

Since the sum of the *n+1* probabilities for the possible states must be equal to *1*, solving for P_0 we get:

$$P_0 = \frac{1}{1 + \sum_{n=1}^{Q} X_n} \tag{3}$$

Once P_0 is known, all the state probabilities P_n can be obtained by using P_0 and the X_n factors, which are obtained from the arrival probability using equation (2).

State probabilities P_n are given by the following equation:

$$P_n = P_0 \sum_{i=1}^{Q} X_i \tag{4}$$

By means of the state probabilities, the required performance parameters can be obtained; for example: *average delay*, *cell loss probability* and *throughput*.

According to equation (4), the *average number of cells in the queue* (E[n]) is given by:

$$E[n] = \sum_{n=0}^{Q} n \left[P_0 \sum_{i=1}^{Q} X_i \right] \tag{5}$$

When establishing the queue capacity it is important to know the probability of loss P_L that is given by:

$$P_L = \sum_{n=0}^{Q} \left[P_n \sum_{i=Q-n+1}^{\infty} A_i \right] \tag{6}$$

Applying Little's equation, the average delay in the queue can be written as:

$$E[W] = \frac{E[Q]}{\lambda} = \frac{E[n] - \rho}{\lambda} \quad , \tag{7}$$

where:

- E[W] : average delay in the buffer.
- E[Q] : average number of cells in the buffer.
- λ : average arrival rate.
- μ : average service rate.
- ρ : utilization factor = λ/μ.

Finally, the total delay (E(T)) is the waiting time in the queue plus the transmission time for the packet.

3.1 Random arrivals with Poisson distribution

The arrival process is considered Poisson if the number of arrivals in a time interval is independent of the arrivals in any other interval, and the number of sources is great. In the case of arrivals with Poisson distribution, the probability of occurrence for exactly *n* arrivals during a time period is given by [9]:

$$A_n(t) = \frac{(\lambda t)^n}{n!} e^{-\lambda t} = \frac{\rho^n}{n!} e^{-\rho} \text{ ; for } n=0,1,2,.. \quad , \tag{8}$$

where:
t : time period, therefore $t = T_c = 1/\mu$.
n : number of arrivals in interval *t*.

For a switch with N input ports, it is considered that all ports receive packets with the same distribution and that the probability that a specific cell arrives through a particular port is the same for all ports and equal to: $p = 1/N$. Therefore, the system can be described as the sum of N Poisson processes with an arrival rate of λN . As expected, the arrival rate for a single port is equal to λ.

For this distribution, the state probability is found by solving equation (1) for $A_n(t)$. Knowing the state probability P_n it is then possible to obtain the loss probability for the Poisson case, given by the following equation:

$$P_L = \sum_{n=0}^{Q}\left[P_n \sum_{i=Q-n+1}^{\infty}\left(\frac{\rho^i}{i!}e^{-\rho}\right)\right] \tag{9}$$

Another parameter of interest is *the average delay in the queue-server system* (E[T]), that is obtained using equation (7) and the Pollaczek-Khinchin equation -see [10]-, this delay is given by equation 10.

$$E[T] = \frac{E[n]}{\lambda} \tag{10}$$

3.2 Random arrivals with Binomial distribution.

The Binomial distribution provides a random number of successes in a certain number of independent attempts, with a given probability of success. If in each time slot (equal to a bus cycle), a packet arrives at each input independently with probability ρ, and each such packet is equally likely destined for each output, the probability (A_k) of *k* packets arriving in a time slot, all destined for a given output, has the following probability distribution:

$$A_n(t) = \left(\frac{N}{n}\right)\left(1-\frac{\lambda t}{N}\right)^{N-n}\left(\frac{\lambda t}{N}\right)^n ; n \le N \quad , \tag{11}$$

where N is the number of ports.

The success probability for each port is given by ρ/N since it is considered that the utilization factor of the complete system is ρ. The state probability is obtained substituting the equation (11) in equation (1). Knowing the state probability, the loss probability for the binomial distribution is obtained, as given by the following equation.

$$P_L = \sum_{n=Q-N+1}^{Q}\left[P_n \sum_{i=Q-n+1}^{N} A_i\right] \tag{12}$$

Also, the average delay in the queue is obtained from equation (7), but in this case the Pollaczek-Khinchin equation can not be used since this is used only for arrivals with Poisson distribution; therefore, it is left in terms of P_0 .

4. SIMULATION AND ANALYSIS OF RESULTS

In this section, a simulation model (which gives a more accurate representation of the switch operation) is presented, it implements the main blocks of the switch fabric. This model is developed using a simulation program called OPNET [12]. The performance parameters, as well as the effect that different algorithms for the bus assignment have on the cell loss probability, are evaluated. For this purpose, the mentioned algorithms were written in C language, and implemented in the simulation model.

The simulation process is performed by changing the frame length (L), the output queue size (Q) and the utilization factor (ρ). Also the efficiency for the bus allocation algorithms is evaluated, namely the fixed and rotating allocation sequences.

The parameters to evaluate in this model are:

- Cell Loss Rate.
- Throughput.
- Average Queuing Delay

4.1 Cell Loss Rate(CLR)

The cell loss rate represents a measure of the probability that a cell is not successfully transmitted to its corresponding output queue. It is obtained at the service stage by the following equation:

$$CLR = \frac{Transmitted \quad cells - received \quad cells}{transmitted \quad cells} \tag{13}$$

Furthermore the success rate, the opposite of the loss rate, is obtained. This represents the probability that a cell is received successfully in its corresponding output queue.

From the results, it can be proved that the sum of the loss factor and the success factor is equal to 1, satisfying the probability property.

Other observed behavior is the increase in the losses (LF) as the utilization factor (ρ) increases, assuming that L and QS remain constant. This is because, with a greater offered load, the inter-arrival time is smaller, so more frames are generated and the queue becomes congested faster. The same effect is present when the queue size is reduced (with a constant offered load) because less memory space will be available for storing an incoming packet.

Note that an increase in the number of cells is also present with longer frames because these are spliced into several cells. Since these frames arrive in bursts to the queue, more losses are present for longer frame sizes. This behavior is shown in figure 2.

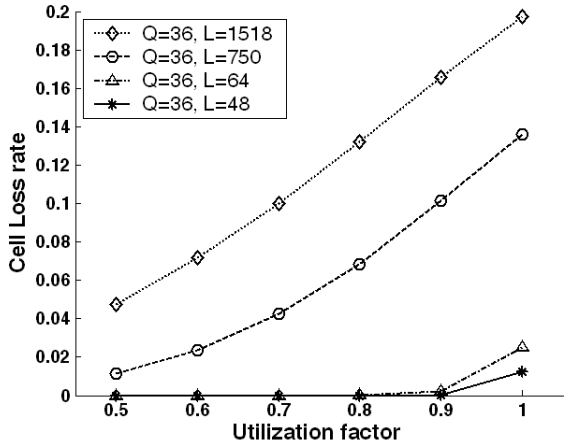

Figure 2. Cell Loss Rate as a function of ρ

In order to compare the simulation results with those obtained by the analytical model, the parameters and assumptions must be the same for both models. The analytical model considers that each frame generates only 1 cell, that is, the frame size is equal to that of the payload (48 *bytes*) in an ATM cell. The inter-arrival time is obtained under this restriction, so the simulation model must adapt to this by generating frames 48-bytes in length, which is smaller than the minimum Ethernet frame length (64 bytes) adding the 8 remaining bytes in the Line Circuit LC when formatting the cell to the switch format.

Note that during the simulation time 10^6 cells are created, but some analytical cases produce losses in the order of 10^8, so the simulation model will not detect those losses and therefore the results can not be compared. To observe losses in the 10^8 order it is necessary to generate at least 10^9 cells, which would be computationally intensive, with impractical simulation times, so these cases were not addressed.

Table 1 shows the results obtained by *analytical* (using Poisson) and *simulation models* as well as *theoretical results* reported in [13]. It can be seen that the simulation results are more optimistic, since the loss is smaller, however, the difference is less than one order of magnitude.

Table I. Comparison of the theoretical, simulation and analytical results.

Q	ρ	Theory [13]	Simulation	Analysis
18	0.7	1.0e-6	1.0e-6	1.02e-6
18	0.8	2.0e-4	1.25e-4	5.84e-5
18	0.9	6.0e-2	2.6e-3	1.74e-3
36	0.7	4.0e-9	<e-6	5.36e-12
36	0.8	6.0e-7	<e-6	2.5e-8
36	0.9	2.0e-4	6.2e-5	4.1e-5

It can also be observed from the simulation results that the success rate (SR) decreases with the increase in the utilization factor (ρ), and the frame length (L), and also by decreasing the queue capacity (QS).

4.2 Throughput

Throughput is a performance parameter that measures the system efficiency through the ratio of the carried traffic and the maximum traffic that can be handled. This parameter is obtained in the service stage using the equation (14):

$$Throughput = \frac{Number\ \ of\ \ served\ \ cells}{Total\ \ cells\ \ in\ \ a\ \ simulation} \tag{14}$$

From the simulation results it is possible to observe that the throughput increases with the utilization factor and that this effect is greater when the queue size is increased. It is also observed that the maximum throughput reached for frame length L = 1518 bytes, is approximately 80%. Another important behavior is the increase in the throughput with longer frames (L), this is because longer frames generate more cells, so the inter-arrival times are smaller, close to the service time for greater offered load (see figure 3).

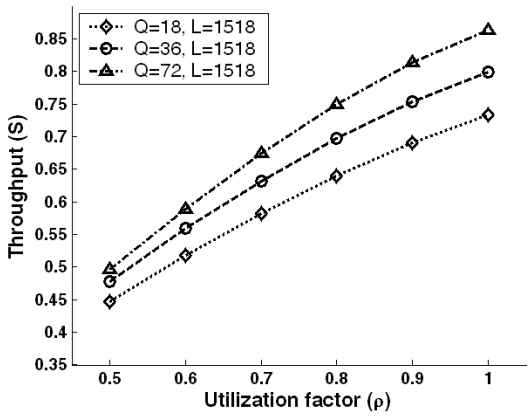

Figure 3. Throughput as a function of ρ

4.3 Average Queuing Delay

The average queuing delay is another important performance parameter in communications systems, mainly when these are for transmission of voice or video.

There is a compromise between the average delay and the loss probability, for example, for data transmission the delay of one packet is not critical, but the complete reception of the packets it is. The opposite case appears in voice transmission, where the delay is a very important factor, while a small data error does not corrupt the entire conversation. The simulation program (OPNET) provides a measure of the average delay for the systems under simulation [12].

Figure 4 shows the results obtained for the *average delay*, where it can be observed an increase in the average delay with an increase in the queue capacity. This is because with a larger queue capacity there are more cells in front of the n-th cell that arrives to the output port, so the cell has to wait for the n-1 cells before it can be served. Another important result is that, while for frames of length L = 48 bytes, the average delay increases in the same way (until ρ = 0.9) for all the 3 queue sizes; this increase is bigger for the queue size equal to 72 for the case of frame length corresponding to L = 1518 bytes. This difference in results is because the frame length of 48 produces just one cell, while the 1518-bytes frame produces a burst of 32 cells.

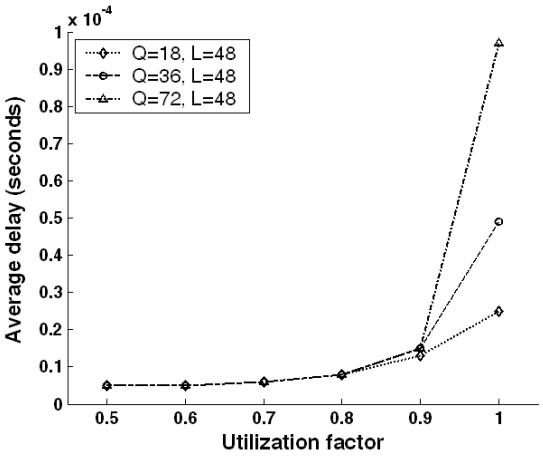

Figure 4. Average Queuing delay, L = 48, varying Q

The average delay increases almost linearly as a function of the utilization factor for frame lengths of 1518 and 750 bytes, but for frames lengths of 64 and 48 bytes the increase is in exponential form, like the distribution of inter-arrival times for these frames, as shown in figure 5. This is because the line circuit (LC) is modeled as an infinite buffer that captures the generated frames and later sends them to the input queue (IQ). For frames of length L = 48 and L = 64 only 1 and 2 cells are generated and these go through the LC with a small delay, giving an output rate similar to that for the incoming frames, which is exponentially distributed. However, with longer frames (L = 1518 and L = 750), there are 32 and 16 (respectively) cells that are simultaneously stored in the LC, but are transmitted to the input queue (IQ) one at a time, with a delay that depends on the frame size. Also, note that regardless of the frame length, the average delay is constant when the utilization factor (ρ) is close to 1; this is because with a greater load the LC stores more cells independently of the frame size.

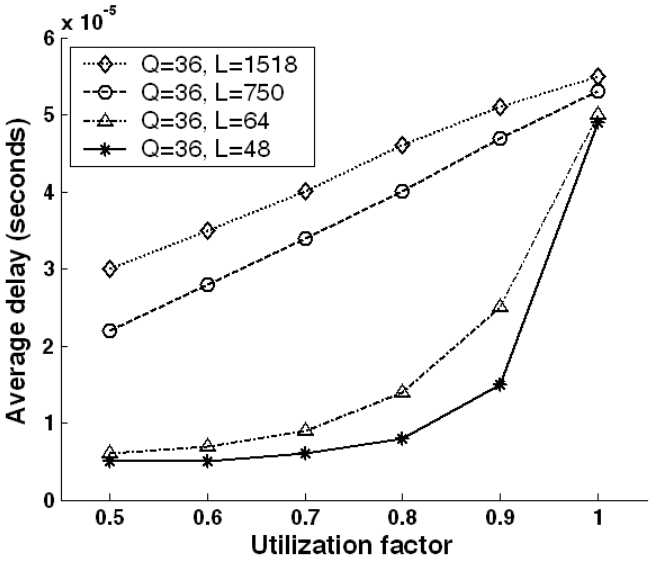

Figure 5. Average Queuing delay, Q = 36, varying L

4.4 Comparison of Bus Assignment Algorithms

In the switch fabric development process, three bus assignment algorithms were analyzed: the dynamic, the fixed start, and the rotating start cyclic algorithms. The later was selected and implemented on the switch. In this section the results obtained by the second and third algorithms are compared and the differences between them are analyzed.

Both algorithms were implemented and tested in the simulation model routing the cells from all the input ports to one output port. As shown in figure 6, the number of lost packets for the cyclic bus assignment algorithm are approximately constant for all ports; while for the rotating cyclic algorithm, the losses are bigger for input ports of increasing index.

Another simulation was developed for both algorithms, changing the destination of cells from a single output port, to a randomly selected output port, choosing the destination sink with a uniform distribution. The results closely resembled those presented in figure 6.

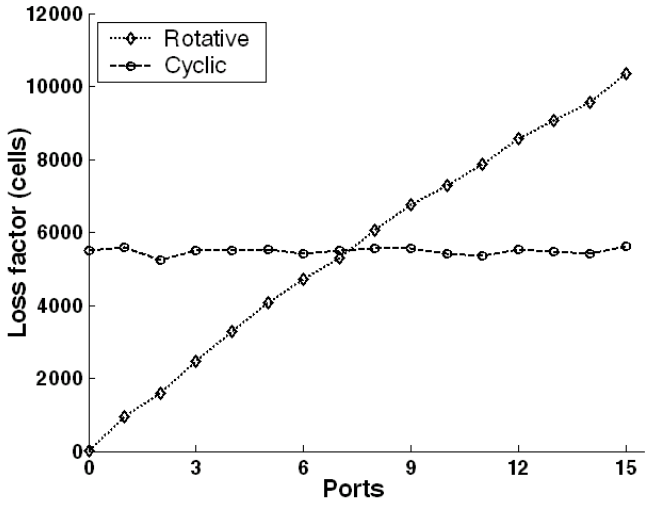

Figure 6. Comparison of the Bus Assignment Algorithm

5. CONCLUSIONS

When comparing the analytical results obtained by formulas with the simulation results, a similar behavior was observed. The simulation results were also compared to results of akin models reported by Tobagi in [13], which were used as reference for the design and dimensioning of the SF, verifying that the SF satisfies the design requirements.

According to the simulation results, the SF presents greater losses in the following cases: when increasing the offered load, when reducing the capacity of the output queues, and when transmitting frames of longer length. On the other hand the throughput of the system increases with the offered load, with queues of big capacity, and with longer frames. It was also observed that the average delay increases with larger queues. Also, when increasing the offered load, the average delay increases linearly for longer frames, while the increment is exponential for small frames.

Furthermore, from simulation results we conclude that the *rotating cyclic algorithm*, provides a more equitable service to the input ports than the *fixed* cyclic algorithm, because the losses in the later one are not uniform for all the ports (where high index ports have greater losses than low index ports). Nevertheless by using the rotating algorithm the losses are approximately equal for all the input ports, even when these losses are larger than the minimum loss present in the fixed cyclic algorithm.

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