# ENHANCING THE SYMBOLIC ANALYSIS OF ANALOG CIRCUITS 

E. Tlelo-Cuautle \& J. Agula-Meza

INAOE, Department of Electronics. Instituto Tecnológico de Puebla. Puebla, Pue., México. etlelo@inaoep.mx

Received: February 2nd ${ }^{\text {nd }}$ 2005. Accepted: April $12^{\text {st }}, 2005$

## ABSTRACT

A new symbolic-method is introduced to enhance the calculation of symbolic expressions of analog circuits. First, the analog circuit is transformed to a nullor equivalent circuit. Second, a new method is introduced to the formulation of a compact system of equations (CSEs). Third, a new method is introduced to the solution of the CSEs, by avoiding multiplications by zero to improve the evaluation of determinants. Finally, two examples are given to show the usefulness of the proposed methods to calculate fully symbolic transfer functions.

## RESUMEN

Se presenta un nuevo método simbólico para mejorar el cálculo de expresiones simbólicas de circuitos analógicos. En primer luğar, el circuito analógico es transformado a un circuito equivalente con anulador (nullor). Segundo, se presenta un nuevo método para la formulación de un sistema de ecuaciones compacto (SEC). Tercero, se presenta un nuevo método para la solución del SEC, evitando multiplicaciones por cero para mejorar la solución de determinantes. Finalmente, se presentan dos ejemplos para mostrar la utilidad de los métodos propuestos para calcular funciones de transferencia totalmente simbólicas.

KEYWORDS: Circult Theory, Symbolic Analysis, Nodal Analysis, Operational Amplifier, Operational TransConductance Amplifier, Nullor, Cartesian Product, Linear Algebra.

## 1. INTRODUCTION

The goal of symbolic analysis is focused on the calculation of symbolic expressions [1-7] to help the designers to gain insight and understanding of the behavior of a circuit. The symbolic expressions should represent the dominant behavior of a circuit to be useful for synthesis and optimization procedures. Furthermore, by applying matrix-methods, four basic procedures are executed, namely: modeling of the circuit elements, formulation and solution of network equations, and simplification of a symbolic expression. On one hand, the majority of symbolic simulators are based on the modified nodal analysis (MNA) method for the formulation of network equations [1-7], which means that controlled sources form the basic set of primitive elements to model the behavior of the analog circuit. The solution of the network equations is done basically by applying Cramer's rule. On the other hand, by modeling the behavior of an analog circuit by using nullors [8], the formulation of network equations can be done by applying nodal analysis (NA) [9-11]. Most important is that the application of the NA method to nullor circuits leads us to formulate a compact system of equations (CSEs) [12]. In this manner, both operations -the formulation of huge matrices and stamping of controlled sources- can be avoided. Henceforth, a new method is introduced to the formulation of a CSEs for analog circuits, by avoiding cumbersome matrix-manipulations. In the same manner, as new contributions for the solution of network equations are based on determinant decision diagrams (DDDs) [13-15], where DDDs use the contents of the
admittance matrix, a new method is also introduced for the solution of the CSEs to enhance the calculation of a fully symbolic expression.

## 2. NULLOR EQUIVALENTS OF ANALOG CIRCUITS

The behavior of any active device and non-NA compatible circuit-element can be modeled by combining nullators and norators [1-2, 8-12]. The nullator is an element which does not allow current through it, and the voltage across its terminals is zero. The norator is an element for which an arbitrary voltage can exist across it and simultaneously an arbitrary current can flow through it. A nullator-norator pair forms the nullor element, which can be used to model the behavior of several analog circuits [8-12], as shown in Figure 1. In this manner, a nullor equivalent circuit can be analyzed by applying the NA method, which consist on formulating equation (1), with: /as the vector of independent current sources, $v$ the vector of node-voltages variables, and $\gamma$ the linear admittance matrix

$$
i=Y v
$$


(a)


(b)


(d)

Figure 1. Nullor equivalents of the (a) independent voltage source, (b) BJT and MOSFET, (c) operational amplifier (OPAMP) and (d) operational transconductance amplifier (OTA)

## 3. FORMULATION OF A COMPACT SYSTEM OF EQUATIONS

For a nullor equivalent circuit, the formulation of its CSEs, having the form of equation (2), can be done by manipulation of the interconnection relationships (IRs) of norators, nullators and admittances. The order of the CSEs $(\mathrm{m})$, is determined by the number of nodes $(\mathrm{n})$ (with the reference node labeled by 0 ), minus the number of nullors (N).

$$
\begin{equation*}
i_{C N A}=Y_{C N A} v_{C N A} \tag{2}
\end{equation*}
$$

The conventional formulation of a CSEs of nullor circuits, by applying the NA method, has been done by the formulation of an initial non-CSEs of order $n$, which is reduced further in one order for each nullor until obtaining a CSEs of order $m=n-N$ [9-11]. It clearly results that this matrix-reduction process implies cumbersome matrix-
manipulations to eliminate $N$ rows and $N$ columns. Furthermore, to avoid complex matrix manipulations, this paper presents a new method to formulate the CSEs of nullor circuits by manipulation of the IRs of norators, nullators and admittances. Henceforth, from the net-list of a nullor equivalent circuit, the proposed formulation method is summarized as follows:

Step Generate three data structures to represent the IRs of:
1 Norators: Generate a set to include the pair of nodes (i,j), associated to each norator $P_{k}$. From the properties of the norator [9], both nodes $i$ and $j$ are virtually short-circuited and those indexes are associated to rows in equation (2).
Nullators: Generate a set to include the pair of nodes $(i, j)$, associated to each nullator $O_{k}$. From the properties of the nullator [9], both nodes $i$ and $j$ are virtually short-circuited and those indexes are associated to columns in equation (2).
3. Admittances: Generate a set containing the symbol and the pair of nodes ( $\mathrm{i}, \mathrm{j}$ ), associated to each admittance.

Step 2. Calculate the indexes associated to rows, columns, and admittances to formulate equation (2) by manipulation of the IRs calculated in step 1.

1 Set ROWIx: It contains m elements ordered numerically, which are calculated by using the IRs and property of the norator, and by including all nodes $n$. These indexes are used to fill vector $i_{C N A}$ in equation (2), and to calculate row-indexes to fill the matrix $Y_{C N A}$
2. Set COLIX: It contains m elements ordered numerically, which are calculated by using the IRs and property of the nullator, and by including all nodes $n$. These indexes are used to fill vector $\boldsymbol{v}_{C N A}$ in equation (2), and to calculate column-Indexes to fill the matrix $Y_{C N A}$

Admittance indexes: They are structured as shown in Table I, by using ROWIx and IRs of admittances. Each element in ROWIx is equated to node $i$, then node-value is equated to node $j$ for each pair of nodes ( $i, j$ ) of each admittance-symbol. Note that always $\mathbf{i} \neq \mathbf{j}$.

Table I. Admittance indexes

| ROWIx | Node | Value | Admittance | Symbol |
| :---: | :---: | :---: | :---: | :---: |
| 1 | $-(0: \mathrm{G} 1)$ | $(4: \mathrm{sC} 3)$ |  |  |
| 2 | $(1: \mathrm{G} 4)$ | $(4: \mathrm{sC} 3$ | $\ldots$ | $(\mathrm{n}-3: \mathrm{G} 7)$ |
| $\vdots$ | $\vdots$ | $\vdots$ | $\ddots$ | $\vdots$ |
| n | $(3: \mathrm{G} 2)$ | $(5: \mathrm{sC} 1)$ | $\ldots$ | $(\mathrm{n}-1: \mathrm{G} 3)$ |

Step 3. Evaluate the Cartesian product among sets ROWIx and COLIx to form pairs of indexes ( $r, c$ ) [16]. Each pair is associated to one symbol in Table $\mathrm{I}: \mathrm{r}$ is searched in ROWIx, then c is searched in node-value until the associated admittance-symbol is found. If $c$ does not exist, the associated value to the pair $(r, c)$ is equated to 0 . Thus, one is able to fill matrix $Y_{C N A}$ in the formulation of equation (2).

## 4. SOLUTION OF NETWORK EQUATIONS

The solution of equation (2) can be obtained by applying Cramer's rule. However, on one hand, since for large circuits the matrices are too sparse, an efficient method should be appled to eliminate multiplications by 0 , e.g. DDDs. On the other hand, since DDDs need to construct a graph to expand the determinant, they spent computational time to
verify the graph-connectivity [13-15]. Furthermore, a new method is introduced herein to avoid both the construction of a graph and multiplications by 0 . It is worth to mention that instead of doing the formulation of matrix $Y_{C N A}$, the proposed method uses its contents by beginning from the admittances calculated in step 3 of section 3, being summarized as follows:

Step 1. Generate a data structure to represent the multiplications for the calculation of the determinant of matrix $Y_{C N A}$ of order m . It is done as follows:

1 Elements of the data structure: For a matrix with all its elements different to 0 , the data structure is an array with m ! rows and m columns.
2. To fill the data structure, one should include element by element as it is done by applying Cramer's rule. So that for the matrix shown in equation (3), the data structure is listed by Table II. According to the previous item. It has $4!\times 4=96$ elements.

Step 2. Evaluate the determinant of the associated matrix by multiplying all the elements of each row in Table II. It is done as follows:

Each element in Table II has been signed according to the evaluation of minors, as it is done by applying Cramer's rule.
For each row, multiply all elements and signs in order to evaluate m! multiplications for a matrix with all its elements different from 0 . So that from Table II, the determinant of equation (3) has $4!=24$ product-terms of 4 elements of the associated matrix.

$$
\left[\begin{array}{llll}
a & b & \ddots & d \\
e & f & \ddots & h \\
i & j & \ddots & l \\
m & n & \ddots & p
\end{array}\right.
$$

Table II. Data structure of equation (3)

| A | f | k | p |
| :---: | :---: | :---: | :---: |
| A | $f$ | -1 | 0 |
| A | -g | $j$ | p |
| A | -g | -1 | n |
| A | h | j | 0 |
| A | h | -k | n |
| -b | - | k | p |
| -b | - | - | 0 |
| -b | 8 | 1 | p |
| -b | g | - 1 | m |
| -b | -h | 1 | 0 |
| -b | -h | -k | m |
| C | e | 1 | p |
| C | e | -1 | n |
| C | -f | 1 | p |
| C | -f | -1 | m |
| C | h | i | n |
| C | h | - | m |
| -d | -e | j | 0 |
| -d | - | -k | n |
| -d | f | 1 | 0 |
| -d | f | -k | n |
| -d | -8 | 1 | n |
| -d | - | - | m |

Step 3. Factorization of a symbolic expression: In Table II, one can identify minors and one can make factorizations composed of two elements. Example: for the rows 1 and 2 the product af is factorized along with the minor kp-lo, which also appears at rows 7 and 8, factorized with the product -be, so that the product-terms for rows 1,2,7,8, can be factorized as (af-be)(kp-lo). The final expression can be factorized as-(af-be)(kp-lo)+(ce-ag) (jp-ln)+(ah-de)(jokn)+(bg-$\mathrm{cf})(\mathrm{ip}-\mathrm{lm})+(\mathrm{df}-\mathrm{bh})(\mathrm{io}-\mathrm{km})+(\mathrm{ch}-\mathrm{dg})(\mathrm{in}-\mathrm{jm})$. It is worth to mention that for sparse matrices, this method avoids multiplications by 0 , as shown in the following section.

## 5. CALCULATION OF FULLY SYMBOLIC EXPRESSIONS

Two examples are presented in this section to calculate their symbolic transfer functions.

### 5.1 Active RC filter

Let's consider the active RC filter taken from page 955 of [5]. By transforming the voltage source and all opamps, the nullor equivalent circuit is shown in figure 2.


Figure 2 Nullor equivalent circuit of the RC filter taken from page 955 of [5]

### 5.1.1 Formulation os the CSEs

Step The data structures of the IRs for norators, nullators and admittances are given by:
IRs of norators: $\{(2,0),(4,0),(6,0),(8,0),(11,0)\}$
IRs of nullators: $\{(1,2),(3,0),(5,0),(7,0),(9,10)\}$
IRs admittances:
$\{[1,(1,0)],[G 1,(2,3)],[S C 1,(3,4)],[G 5,(3,4)],[G 4,(4,5)],[G 3,(4,10)],[G 7,(5,6)],[G 8,(6,7)],[G 6,(3,8)],[5 C 2,(7,8)],[G 2,(2,10$ )],[G9,(8,9)],[G10,(9,0)],[G11,(10,11)]].

Step 2. The indexes associated to rows, columns, and admittances are given by:
Set ROWIx: $\{(1),(3),(5),(7),(9),(10)\}$. By using these indexes $i_{C N A}=\left[v_{i n}, 0,0,0,0,0\right]^{t}$.
) Set COLIx: $\{(1,2),(4),(6),(8),(9,10),(11)\}$. From which $v_{C N A}=\left[v_{1,2}, v_{4}, v_{6}, v_{8}, v_{9,10}, v_{11}\right]^{\}}$.
3. Admittance indexes: They are searched in the IRs of admittances. The search is only done for the indexes included in ROWIx. as shown in Table III.

| ROWIx | (Node: symbol) |
| :---: | :---: |
| 1 | (0: 1) |
| 3 | (2: G1) (4: sCl) (4: G5) (8: G6) |
| 5 | (4: G4) (6: G7) |
| 7 | (6: G8) (8: sC2) |
| 9 | (8: G9) (0: G10) |
| 10 | (4: G3) (2: G2) (11: G11) |
|  |  |

Step 3. The Cartesian product ROWIx×COLIx is given by equation (4).

$$
\left[\begin{array}{cccccc}
(1,1)+(1,2) & (1,4) & (1,6) & (1,8) & (1,9)+(1,10) & (1,11)  \tag{4}\\
(3,1)+(3,2) & (3,4) & (3,6) & (3,8) & (3,9)+(3,10) & (3,11) \\
(5,1)+(5,2) & (5,4) & (5,6) & (5,8) & (5,9)+(5,10) & (5,11) \\
(7,1)+(7,2) & (7,4) & (7,6) & (7,8) & (7,9)+(7,10) & (7,11) \\
(9,1)+(9,2) & (9,4) & (9,6) & (9,8) & (9,9)+(9,10) & (9,11) \\
(10.1)+(10.2) & (10,4) & (10,6) & (10,8) & (10,9)+(10,10) & (10,11)
\end{array}\right]
$$

As one sees, it generates pairs ( $(\mathrm{r}, \mathrm{c}$ ) associated to an admittance symbol which is searched in Table III. For $\mathrm{r}=\mathrm{c}$, one should add all symbols in the row associated to index $r$ from column ROWIX. For example, for $\mathrm{Y} 65=(10,9)+(10,10)$ : $\mathrm{r} 1=10$ is located at the end of ROWIX in Table III. Now, by searching for $\mathrm{c} 1=9$, it results that c 1 has not any associated symbol, therefore ( 10,9 ) $=0$. However, for the next pair $\mathrm{r} 2=\mathrm{c} 2=10$, this means that all admittances associated to r 2 should be added, so that: $(10,10)=G 3+G 2+G 11$. Furthermore, by evaluating all the pairs $(r, c)$, the resulting CSEs is given by equation (5).

$$
\left|\begin{array}{c}
v_{\text {in }}  \tag{5}\\
0 \\
0 \\
0 \\
0 \\
0
\end{array}\right|=\left[\begin{array}{cccccc}
1 & 0 & 0 & 0 & 0 & 0 \\
-G 1 & -G 5-s C 1 & 0 & -G 6 & 0 & 0 \\
0 & -G 4 & -G 7 & 0 & 0 & 0 \\
0 & 0 & -G 8 & -s C 2 & 0 & 0 \\
0 & 0 & 0 & -G 9 & G 9+G 10 & 0 \\
-G 2 & -G 3 & 0 & 0 & G 2+G 3+G 11 & -G 11
\end{array}\right]\left[\begin{array}{c}
v_{1,2} \\
v_{4} \\
v_{6} \\
v_{8} \\
v_{9,10} \\
v_{11}
\end{array}\right]
$$

### 5.1.2 Calculation of the fully symbolic transfer function (FSIF)

By applying the proposed solution method, the FSTF can be calculated as follows:
Step 1. Generation of the data structure:
In equation (5), only $39 \%$ of the elements are different from 0 , this means that the data structure will be an array with very few rows than m ! and m columns.
2. By including element by element as it is done by applying Cramer's rule, the data structure is listed in Table IV.

Step 2. Evaluation of the determinant by multiplication of all the elements in each row:
Each element in Table IV is calculated according to the evaluation of minors by applying Cramer's rule. However, the generation of rows is stopped if an element of the determinant equals to zero, so that many savings result compared to Cramer's rule, and also there is not a need to generate an associated graph, as it is done by DDDs. Furthermore, only 23 rows were generated in Table IV, instead of m!=6!=720 if the matrix $Y_{C N A}$ were not sparse.
2. For each row with all its $m$ elements different of zero, multiply all the admittance elements and signs. So that from Table IV, only 2 multiplications arise, those in rows 1 and 10 . The determinant of equation (5) is thus given by equation (6).

$$
\Delta Y_{C N A}=\left(\mathrm{Y} 11^{*} Y 22^{*} \mathrm{Y} 33^{*} \mathrm{Y} 44^{*} \mathrm{Y} 55^{*} \mathrm{Y} 66\right)+\left(\mathrm{Y} 11^{*} \mathrm{Y} 24^{*} Y 32^{*} Y 43^{*} \mathrm{Y} 55^{*} \mathrm{Y} 66\right)
$$

Table IV. Data structure to calculate the determinant of equation (5)

| $Y 11$ | $Y 22$ | $Y 33$ | $Y 44$ | $Y 55$ | $Y 66$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $Y 11$ | $Y 22$ | $Y 33$ | $Y 44$ | 056 |  |
| $Y 11$ | $Y 22$ | $Y 33$ | 045 |  |  |
| $Y 11$ | $Y 22$ | $Y 33$ | 046 |  |  |
| $Y 11$ | $Y 22$ | 034 |  |  |  |
| $Y 11$ | $Y 22$ | 035 |  |  |  |
| $Y 11$ | $Y 22$ | 036 |  |  |  |
| $Y 11$ | 023 |  |  |  |  |
| $Y 11$ | $Y 24$ | $Y 32$ | 041 |  |  |
| $Y 11$ | $Y 24$ | $Y 32$ | $Y 43$ | $Y 55$ | $Y 66$ |
| $Y 11$ | $Y 24$ | $Y 32$ | $Y 43$ | 056 |  |
| $Y 11$ | $Y 24$ | $-Y 33$ | 042 |  |  |
| $Y 11$ | $Y 24$ | $-Y 33$ | 045 |  |  |
| $Y 11$ | $Y 24$ | $-Y 33$ | 046 |  |  |
| $Y 11$ | $Y 24$ | 035 |  |  |  |
| $Y 11$ | $Y 24$ | 036 |  |  |  |
| $Y 11$ | 025 |  |  |  |  |
| $Y 11$ | 026 |  |  |  |  |
| 012 |  |  |  |  |  |
| 013 |  |  |  |  |  |
| 014 |  |  |  |  |  |
| 015 |  |  |  |  |  |
| 016 |  |  |  |  |  |

Step 3. Factorization procedure: Equation (6) can be factorized as shown by equation (7).

$$
\begin{equation*}
\Delta Y_{C N A}=\mathrm{Y} 11 * \mathrm{Y} 55 * \mathrm{Y} 66 *(\mathrm{Y} 22 * \mathrm{Y} 33 * \mathrm{Y} 44+\mathrm{Y} 24 * \mathrm{Y} 32 * \mathrm{Y} 43) \tag{7}
\end{equation*}
$$

By replacing each admittance $Y_{i j}$ by its corresponding symbols from equation (5), then equation (7) becomes equation (8), where by multiplying all the elements, the resulting simplified determinant is given by equation (9). Furthermore, after the solution for $v_{\text {out }}=v_{11}$, the FSTF is given by equation (10), according [5].

$$
\begin{equation*}
\Delta Y_{C N A}=(1)(\mathrm{G} 9+\mathrm{G} 10)(-\mathrm{G} 11)[(-\mathrm{G} 5-\mathrm{sC} 1)(-\mathrm{G} 7)(-\mathrm{sC} 2)+(-\mathrm{G} 6)(-\mathrm{G} 4)(-\mathrm{G} 8)] \tag{8}
\end{equation*}
$$

$$
\Delta Y_{C N A}=\mathrm{G} 11(\mathrm{G} 9+\mathrm{G} 10)\left[s \mathrm{G} 5 \mathrm{G} 7 \mathrm{C} 2+s^{2} \mathrm{C} 1 \mathrm{G} 7 \mathrm{C} 2+\mathrm{G} 6 \mathrm{G} 4 \mathrm{G} 8\right]
$$

$\frac{v_{11}}{v_{i n}}=\frac{-(G 9+G 10) C 1 G 2 C 2 G 7 s^{2}+((G 1 G 3-G 2 G 5)(G 9+G 10)) C 2 G 7 s-G 4 G 8(G 9 G 1(G 2+G 3+G 11)+G 2 G 6(G 9+G 10))}{G 11(G 9+G 10)\left(G 6 G 8 G 4+s C 2 G 7 G 5+s^{2} C 2 G 7 C 1\right)}$

### 5.2 OTA filter

Let's consider the OTA filter shown in figure 3, its FSTF is calculated as follows:


Figure 3 Nullor equivalent circuit of the OTA filter taken from page 28 of [17]

### 5.2.1 Formulation of the CSEs

Step 1. The IRs of norators and nullators are given by equations (11) and (12).

$$
\begin{align*}
& \{(2,0),(9,3),(10,0),(11,0),(12,3),(13,0),(14,4),(15,4),(16,0),(6,0),(8,0),(17,0),(18,4)\}  \tag{11}\\
& \{(1,2),(9,4),(10,0),(11,2),(12,0),(13,3),(14,0),(5,6),(7,8),(15,4),(16,0),(17,6),(18,0)\} \tag{12}
\end{align*}
$$

RRs of admittances are calculated as: $\{[g m 1,(9,10)],[g m 2,(13,14)],[g m 3,(15,16)]$. [gm4, (17,18)],[gm5,(11,12)],[1,(1,0)],[1,(5,0)],[1,(7,0)],[sC1,(3,0)],[sC2(4,8)]].

Step 2. The admittance indexes are shown in Table V. ROWIx and COLIx are given by:
ROWIX: $\{(1),(3,9,12),(4,14,15,18),(5),(7)\}$. Thus $i_{C N A}=\left[v_{A}, 0,0, v_{B}, v_{C}\right]$
COLIX: $\{(1,2,11),(3,13),(4,9,15),(5,6,17),(7,8)\}$. Thus $v_{C N A}=\left[v_{1,2,11}, v_{3,13}, v_{4,9,15}, v_{5,6,17}, v_{7,8}\right]^{\ddagger}$

Step 3. After the evaluation of ROWI $\times \times$ COLIx, the resulting CSEs is given by Eq. (13).

$$
\left.\left\lvert\, \begin{array}{c}
v_{A}  \tag{13}\\
0 \\
0 \\
v_{B} \\
v_{C}
\end{array}\right.\right]=\left[\begin{array}{ccccc}
1 & 0 & 0 & 0 & 0 \\
-g m 5 & s C 1 & g m 1 & 0 & 0 \\
0 & -g m 2 & s C 2+g m 3 & -g m 4 & -s C 2 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1
\end{array}\right]\left[\left.\begin{array}{c}
v_{1,2,11} \\
v_{3,13} \\
v_{4,9,15} \\
v_{5,6,17} \\
v_{7,8}
\end{array} \right\rvert\,\right.
$$

Table V. Admittance indexes

| ROWIx | (Node: symbol) |
| :---: | :---: |
| 1 | $(0: 1)$ |
| 3 | $(0: \mathrm{sC} 1)$ |
| 9 | $(10: \mathrm{gm} 1)$ |
| 12 | $(11: \mathrm{gm} 5)$ |
| 4 | $(8: \mathrm{sC} 2)$ |
| 14 | $(13: \mathrm{gm} 2)$ |
| 15 | $(16: \mathrm{gm} 3)$ |
| 18 | $(17: \mathrm{gm} 4)$ |
| 5 | $(0: 1)$ |
| 7 | $(0: 1)$ |

### 5.2.2 Calculation of the FSTF

The FSTF is calculated by solving for $\boldsymbol{v}_{\boldsymbol{o}}=\boldsymbol{v}_{4}$. However, as can be seen, this voltage-variable is associated to the solution for $v_{4,9,15}$. For instance, the calculation of the determinant of equation (13), generates the data structure listed in Table VI, for which two multiplications arise, those associated to rows 1 and 7 . Then the determinant is given by equation (14), its factorization by equation (15), and the simplified expression by equation (16).

$$
\begin{gather*}
\Delta Y_{C N A}=Y 11^{*} \mathrm{Y} 22^{*} \mathrm{Y} 33^{*} \mathrm{Y} 44^{*} \mathrm{Y} 55-\mathrm{Y} 11^{*} \mathrm{Y} 23^{*} \mathrm{Y} 32^{*} \mathrm{Y} 44^{*} \mathrm{Y} 55  \tag{14}\\
\Delta Y_{C N A}=\mathrm{Y} 11^{*} \mathrm{Y} 44^{*} \mathrm{Y} 55\left(\mathrm{Y} 22^{*} \mathrm{Y} 33-\mathrm{Y} 23^{*} \mathrm{Y} 32\right)  \tag{15}\\
\Delta Y_{C N A}=  \tag{16}\\
s^{2} C 1 C 2+s C 1 g m 3+g m 1 g m 2
\end{gather*}
$$

Furthermore, after the solution for $v_{4,9,15}$, the FSTF is given by equation (17), see [17].

$$
\begin{equation*}
v_{4,9,15}=\frac{s^{2} C 1 C 2 v_{C}+s C 1 g m 4 v_{B}+g m 2 g m 5 v_{A}}{s^{2} C 1 C 2+s C 1 g m 3+g m 1 g m 2} \tag{17}
\end{equation*}
$$

From these examples, it could be can concluded about the usefulness to be extend the proposed methods to noise analysis of analog circuits, e.g. to improve the method given in [18].

| $Y 11$ | $Y 22$ | $Y 33$ | $Y 44$ | $Y 55$ |
| :--- | :--- | :--- | :--- | :--- |
| $Y 11$ | $Y 22$ | $Y 33$ | 045 |  |
| $Y 11$ | $Y 22$ | $-Y 34$ | 043 |  |
| $Y 11$ | $Y 22$ | $-Y 34$ | 045 |  |
| $Y 11$ | $Y 22$ | $Y 35$ | $-Y 44$ |  |
| $Y 11$ | $Y 22$ | $Y 23$ | $Y 44$ |  |
| $Y 11$ | $-Y 23$ | $Y 32$ | 045 |  |
| $Y 11$ | $-Y 23$ | $Y 44$ | 042 |  |
| $Y 11$ | $-Y 23$ | $-Y 44$ | 045 |  |
| $Y 11$ | 024 |  |  |  |
| $Y 11$ | 025 |  |  |  |
| $Y 11$ |  |  |  |  |
| 012 |  |  |  |  |
| 013 |  |  |  |  |
| 014 |  |  |  |  |
| 015 |  |  |  |  |

## 6. CONCLUSION

Two new methods to enhance the symbolic analysis of analog circuits have been introduced. From the nullor equivalent circuit of an analog circuit, it has been described the manner in which is formulated a CSEs by avoiding complex matrix-manipulations. In the same manner, it has been described the manner in which the solution to a CSEs is done by avoiding both the generation of an associated graph and multiplications by 0 . Furthermore, from the two examples given in section 5, it could be concluded the usefulness of the proposed methods to calculate fully symbolic expressions of analog circuils by the manipulation of the interconnection relationships. Besides, enhanced data structures can be generated for the solution method, by deleting those rows ending by an element equal to 0ij. Most important is that there is no need to formulate equation (2), since the solution method uses the elements calculated from the evaluation of the Cartesian product in section 3. As a final conclusion, the proposed symbolic method is very suitable to be implemented within an environment of analog design automation (ADA), which nowadays is very much needed because ADA has a very large design space in which to operate. So that, one could be able to calculate analytical design equations to deal with constraints such as transfer functions, offset, impedances, nolse, distortion, and several others.

## 7. ACKNOWLEDGMENT

This work has been partially supported by CoSNET/MEXICO, under the project number 454.03-p.

## 8. REFERENCES

[1] Chua. L. O. and Lin P.M., Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, NJ: Prentice-Hall, 1975.
[2] Lin P.M., Studies in Electrical and Electronic Engineering 41: Symbolic Network Analysis, New York: Elsevier, 1991
[3] Fernández, F. V. Symbolic Analysis Techniques. In Applications to Analog Design Automation. The IEEE PRESS, Inc., New York 1998
[4] Rutenbar R. A., Gielen G. and Antao B. A., Computer-Aided Design of Analog Integrated Circuits and Systems, NJ: IEEE Press, 2002.
[5] Toumazou C., Moschytz G. and Barrie G., Trade-offs in analog circuit design, The Netherlands: Kluwer, 2002.
[6] Gielen G., Wambacq P., Sansen W.M., Symbolic analysis methods and applications for analog c tutorial overview, Proceedings of the IEEE, vol. 82, no. 2, pp. 287-304, February 1994.
[7] Hassoun M. M, Pen-Min L., A hierarchical netwntk annenach to symbolic analysis of large-scale netw Transactions on Circuits and Systems-I, vol. 42, no. 4, pp. 201-211, 1995.
[8] H. Schmid, Approximating the universal active element, IEEE [ransactions on Circuits and Systems-1 no. 11, pp. 1160-1169, November 2000.
[9] J. A. Svoboda, Using nullors to analyze linear networks, Circuit Theory and Applications, vol. 14, pp. 1986.
[10] Floberg H. Symbolic analysis in analog integrated circuit design, Norwell, MA: Kuwer, 1997.
[11] Thelo-Cuautle E., Sarmiento-Reyes A., A pure nodal analysis method suitable for analog circuils usin Journal of Applied Research and Technology, vol. 1, no 3 pn 335.747 nctoher 2003.
[12] E. Tlelo-Cuautle, et al., SIASCA: Interactive system for the symbolic analysis of analog circuils, IEICE Express, vol. 1, no. 1, pp. 19-23, April 2004.
[13] C.J. Richard Shi and Xiang-Dong Tan, Canonical symbolic analysis of large analing circuits with det decision diagrams, IEEE Transactions on Computer-Aided Design, vol. 19, no.1, pp. 1-18, January 2000
[14] W. Verhaegen, G. Gielen, Efficient DDD-Based Symbolic Analysis of Linear Analnd Circuits, IEEE Circuits and Systems-II, vol. 49, no. 7, pp. 474-487, July 2002.
[15] Sheldon X.-D. Tan, C.-J. Richard Shi, Efficient approximation of symbolic expressions for analog t modeling and analysis, IEEE Transactions on Computer-Aided Design, vol. 23, no. 6, on an7.018, 200-
[16] Ahmad M. Ibrahim, Introduction to applied fuzzy electronics, Nj: Prentice-Hall, 1997.
[17] Randall L.G., Sánchez-Sinencio E., Active Filter Desiğn Using Operational Trans-conductance An Tutorial, IEEE Circuits and Devices Magazine, pp. 20-32, 1985.
[18] E. Tlelo-Cuautle, C. Sánchez-López, Symbolic computation of NF of transistor circuits, IEICE Trans Fundamentals of Electronics, Communications and Computer Sciences, vol. E87-A, no. 9, pp. September 2004.

Authors Biography


Esteban Tlelo-Cuautle recelved the B.Sc. degree in Flectronirs Englineering from the Tect Institute of Puebla (/nstituto Tecnologico de Puebla), México, in 1993, the M.Sc. and Ph.D. degrees from th Institute for Astrophysics, Optics and Electronics (INAOE), México, in 1995 and 2000, respectively. Since Jar he has been with the Electronics Department at INAOE, where he s rirrently a Researcher. He is Senior A the IEEE, and his research interests include analog design automation, modeling and simulation of nonlinear circuits, symbolic analysis, circult synthesis, and analog and mixed-signal CAD tools.


Jorge Agula-Meza received the B.Sc. degree in Electronics from the Benemerifa $L$ Autónoma de Puebla (BUAP), México, in 2003, and the M.Sc. degree from the National Institute for Ast Optics and Electronics (INAOE), México, in 2004. His research interests include analngue CAD tools, symb analysis, modelling and simulation of analog integrated circuits.

