THE MILLER OPERATIONAL AMPLIFIER'S SETTLING RESPONSE

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ABSTRACT

This paper presents a third-order transfer function to model the settling response of the Miller operational amplifier. The amplifier was simulated (spice) and designed according to design rules of a standard 1.5μm CMOS fabrication process. The proposed mathematical model -based on design parameters under the designer's control- is the best settling approach reported up to now.

KEYWORDS: Modeling, circuit theory, amplifiers.
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1. INTRODUCTION

The Miller operational amplifier, also called opamp, is one of the most important basic blocks for analog signal processing. Filtering applications, A/D and D/A converters, S-H circuits and $\Sigma\Delta$ modulators are some examples of the opamp-based analog applications signal processing. These applications generally correspond to the time domain and that is the reason why time-based modeling was developed as a research field some decades ago. Modeling is important because it constitutes a design tool in the designer's activity. Hence, designers can optimize their design by incorporating additional design parameters or, alternatively, by adding worst case analysis. Once the whole design satisfies given specs, the fabrication of the system is commonly approved. The design process based on modeling is a low-cost activity and widely recommended due to its simplicity.

2. PROBLEM DEFINITION

Fig. 1 shows the CMOS-type Miller opamp, which is composed by a differential input stage and an output gain stage. Here, physical and electrical characteristics of the input transistors are matched (M_{n1} and M_{n2}). By assuming the linear current-voltage characteristic of the MOS transistor, it is easy to demonstrate that the output voltage of the opamp is given by

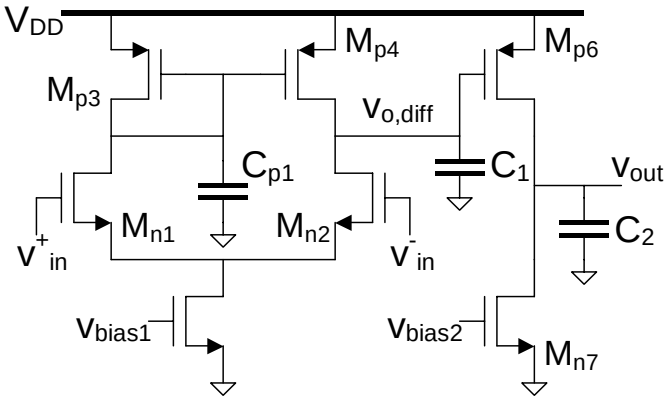


Figure 1. The Miller opamp. Here C_{p1} and C_1 are parasitic capacitances

$$v_{out} = \frac{A_0}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)}(v_{in}^{+} - v_{in}^{-}) \tag{1}$$

where the so-called low-frequency open-loop gain follows

$$A_0 = \frac{g_{mn1}}{g_{dsn1}+g_{dsp4}} \cdot \frac{g_{mp6}}{g_{dsn7}+g_{dsp6}} \tag{2}$$

In this result, $[g_m]$=S and $[g_{ds}]$=S are basic parameters of the MOS transistor [1]. Fig. 1 shows an intrinsic pole ω_{p1} that is due to the parasitic C_{p1} and also to g_{mp3}. Thus, (1) is a valid model if and only if the condition $|s| < g_{mp3}/C_{p1}$ is satisfied. On the other hand, ω_1 is the pole of the input stage given by $(g_{dsp4}+g_{dsn2})/C_1$, while the output pole given by

$$\omega_2 = \frac{g_{dsn7}+g_{dsp6}}{C_2} \tag{3}$$

depends on both the output load (C_2) and the whole output conductance($g_{dsn7}+g_{dsp6}$). From the point of view of circuit analysis, Fig. 2a is a lumped circuit that models accurately to (1). That fact explains why several authors have used that circuit to analyze the settling performance of the Miller opamp. However, the circuit actually models in high percentage just to the non-compensated Opamp. In practice, even when compensation criteria are satisfied, the circuit shown in Fig. 2a does not model accurately the corresponding opamp's performance. Thus, in this paper we demonstrate that an equivalent third-order model not only matches the spice simulation of the lumped equivalent circuit, but also matches the response obtained from spice simulation of the compensated Miller opamp at transistor level

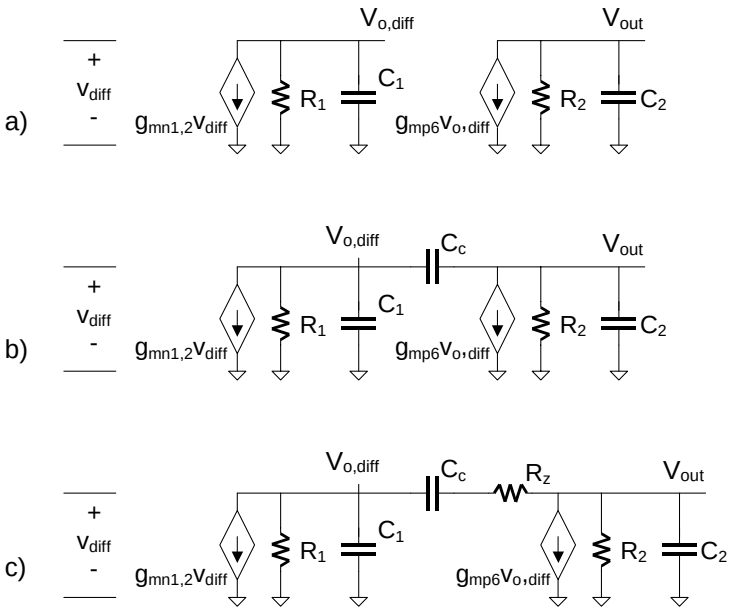


Figure 2. a) Second-order equivalent lumped circuit to model (1); b) equivalent lumped circuit to model a compensated opamp; c) Third-order equivalent lumped circuit to model the Miller opamp including a resistor R_z

3. COMPENSATED OPAMP

When the opamp's phase margin (ϕ) satisfies the condition $45^o<\phi<60^o$, it is well known that stability is satisfied for those cases where the opamp is used in closed-loop configurations; otherwise, it must be correctly compensated. By adding a capacitor (C_c) between both stages, stability would be obtained because the low-frequency pole is moved towards lower frequencies; that procedure is also called the *split-pole technique*. Applying KCL to the circuit shown in Fig. 2b, we found that the transfer function is given by

$$\frac{v_{out}}{v_{diff}} = \frac{R_1 R_2 g_{mn1}(g_{mp6} - sC_c)}{1 + s\left[R_1 R_2 g_{mp6} C_c + R_1(C_1 + C_c) + R_2(C_2 + C_c)\right] + s^2 R_1 R_2 \left(C_2\left[C_1 + C_c\right] + C_c C_1\right)} \tag{4}$$

From this result we can see a zero, which certainly affects the frequency response of the opamp; that is visualized by measuring the margin phase at the 0-db frequency. In order to eliminate the zero effect, a resistor (R_z) is series connected with C_c. Table 1 shows the width of the transistor for each MOS device (see Fig. 1), where the length for all devices is L=3μm. Other useful design parameters are also presented in the same table. Taken into account the equivalent circuit shown in Fig. 2c, we found that the transfer function is given by

$$\left.\frac{v_{out}}{v_{diff}}\right|_{R_z=\frac{1}{gmp6}} = \frac{\frac{g_{mn1}g_{mp6}}{C_1C_2R_zC_c}}{\frac{1}{R_1C_1R_2C_2R_zC_c} + s\frac{1}{C_1R_2C_2R_z}\left[R_2g_{mp6} + \frac{R_z}{R_1} + 2\frac{R_2C_2}{R_1C_c} + \frac{C_1}{C_c} + 1\right] + s^2\frac{1}{R_zC_c}\left[\frac{C_c}{C_1} + \frac{C_c}{C_2} + 1 + \frac{R_zC_c}{R_1C_1}\left(1 + \frac{R_1C_1}{R_2C_2}\right)\right] + s^3}$$

(5)

where the zero is certainly eliminated by proposing $R_z=1/g_{m,p6}$ is proposed. Once the stability is obtained, some authors postulate that a second-order model, equivalent to (1), is a sufficient representation to model the compensated opamp for small-signal linear analysis. Such an approach is not a correct one because, as we can see in (5), the system is actually a third- order model. In fact, the zero effect does not appear any more but R_z plays an important role in the transfer function, where we are assuming that the denominator is modeled by $D(s)=s^3+k_1s^2+k_2s+k_3$, being each constant k_i (i=1, 2, 3) easily deduced with the help of (5).

Device	W (μm)	Parameter	Value
M_{n1} , M_{n2}	87.5	C_c	5.0pF
M_{p3} , M_{p4}, M_{p6}	20.0	C_L	1.0pF
M_{n5}	64.6	V_{DD}	5.0V
M_{n7}	33.0	V_{bias1}, V_{bias2}	1.25V

Table 1 Parameters of the compensated Miller opamp

4. SETTLING ANALYSIS

In order to determine the conditions for a suitable settling analysis, the lumped circuit shown in Fig. 2c - mathematically modeled by (5)- will be analyzed. The root locus analysis indicates that the dominant pole, ω_1, remains almost in the same position as indicated by (1). That is true because that pole is the function of both the Miller capacitance C_m and the resistor R_1:

$$\omega_1 \approx \frac{1}{R_1 C_m} = \frac{1}{g_{mp7} R_2} \cdot \frac{1}{R_1 C_c} \tag{6}$$

On the other hand, Table 2 shows the value of each singularity, while Fig. 3 illustrates spice results. As we can see, there is a frequency f_{max} in which the third-order model fits suitably to the transistor-based response obtained from spice simulations. The advantage of this graphical comparison is that fitting includes the opamp entire frequency range, i.e. from DC to the 0dB gain frequency. The latter will be also useful to show the capabilities of the proposed model. Thus, the time response of the compensated Miller opamp is obtained with the help of the following model:

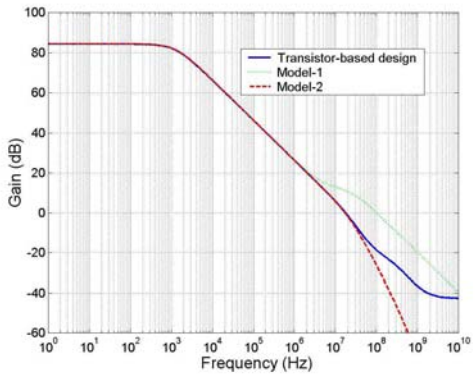


Figure 3. Spice results of the circuits shown in Fig. 2b and 2c, where each one is labeled as Model-1 and Model-2, respectively

Singularity	2nd order model	3rd order model
ω_2	27.7 MHz	557 MHz
ω_1	1.59 kHz	1.25 kHz
z_0	4.8 MHz	32 GHz
ω_3		2.3 GHz

Table 2. Pole/zero values deduced from the equivalent models

$$v_o(t) = \begin{cases} \sum_{i=1}^{3} A_i e^{p_i t} + A_4 t + A_5 , \ 0 \le t \le T_{min} \\ \\ \sum_{i=1}^{3} B_i e^{p_i t} + B_4 , \ t > T_{min} \end{cases} \tag{7}$$

where the constants are calculated from initial conditions. In order to analyze the settling response, in the following the opamp is used in a follower configuration. During the slewing period, the input stage is current limited, which means that the loop works as an open circuit; this period is modeled by (5). Next, by applying the properties of convolution it is possible to deduce, from (5), the following differential equation:

$$\frac{d^3 v_o(t)}{dt^3} + \sum_{i=1}^{2} k_i \frac{d^i v_o(t)}{dt^i} + k_3 v_o(t) = A_o k_3 v_{in}(t) \tag{8}$$

Then, by substituting the input voltage in (8), $v_{in}(t)=v(t)-v_o(t)$, the differential equation of the closed loop configuration is obtained. Next, in a follower configuration the opamp's input voltage is composed by two components: the output response, $v_o(t)$, and the step signal, v(t). Hence, (8) can be rewritten as follows:

$$\frac{d^3 v_o(t)}{dt^3} + \sum_{i=1}^{2} k_i \frac{d^i v_o(t)}{dt^i} + k_3(1 + A_o) v_o(t) = A_o k_3 v(t) \tag{9}$$

As a consequence, to solve the third- order differential equation, the complementary solution follows

$$v_c = \sum_{i=1}^{3} C_i e^{p_i t} \tag{10}$$

where C_i are constants that are obtained also from initial conditions, while p_i are the poles of the system. In this way, poles can be found by solving the following characteristic equation:

$$p_3 + k_1 p^2 + k_2 p + k_3(A_o + 1) = 0 \tag{11}$$

By knowing the poles' values, the general solution is calculated once the step signal is fully described:

$$v(t)=\begin{cases} V_{step}\dfrac{t}{T_{min}}, 0\le t\le T_{min} \\ \\ V_{step}, t\ge T_{min} \end{cases} \tag{12}$$

where V_{step} is the step magnitude, and $T_{min}=1/f_{0dB}$ is the time in which the step signal reaches its final value. Then, since the system's singularities are generally of the following class:

$$\begin{aligned} p_{1,2} &= -\alpha \pm j\beta \\ p_3 &= -\sigma \end{aligned} \tag{13}$$

it is simple to verify that the complementary solution follows

$$v_c(t)=A_1e^{-\sigma t}+e^{-\alpha t}\left[A_2\cos(\beta t)+A_3\sin(\beta t)\right] \tag{14}$$

Since the input signal presents a linear characteristic, see (12), the particular solution must be a first-order solution, or equivalently

$$v_p(s)=A_4t+A_5 \tag{15}$$

In order to obtain the particular solution (15) must be substituted in (9)

$$v_p(t)=\frac{V_{step}}{T_{min}}\cdot\frac{A_o}{A_o+1}\left(t-\frac{k_2}{k_3}\cdot\frac{1}{A_o+1}\right) \tag{16}$$

Thus, the general solution in the rise region, $0\le t\le T_{min}$, is

$$v_o(t)=A_1e^{-\alpha t}+e^{-\alpha t}\left[A_2\cos(\beta t)+A_3\sin(\beta t)\right]+\frac{V_{step}}{T_{min}}\cdot\frac{A_o}{A_o+1}\left(t-\frac{k_2}{k_3}\cdot\frac{1}{A_o+1}\right) \tag{17}$$

where A_i (i=1, 2, 3) are calculated from initial conditions as well:

$$A_1+A_2-\frac{k_2A_oV_{step}}{k_3(A_o+1)^2T_{min}}=v(0) \tag{18-a}$$

$$-\sigma A_1-\alpha A_2+\beta A_3+\frac{A_oV_{step}}{(A_o+1)T_{min}}=v'(0) \tag{18-b}$$

$$\sigma^2A_1+(\alpha^2-\beta^2)A_2-2\alpha\beta A_3=v''(0) \tag{18-c}$$

Furthermore, for $t\ge T_{min}$ the input signal is V_{min}, and the particular solution would be a constant. By assuming $v_c(t)=D_2$, it results that

$$v_c(t)=\frac{A_o}{A_o+1}V_{step} \tag{19}$$

and the general solution for $t\ge T_{min}$ follows

$$v_o(t) = \frac{A_o V_{step}}{A_o + 1} + B_1 e^{-\sigma(t - T_{min})} + e^{-\alpha t}\left[B_2 \cos\beta(t - T_{min}) + B_3 \sin\beta(t - T_{min})\right] \quad (20)$$

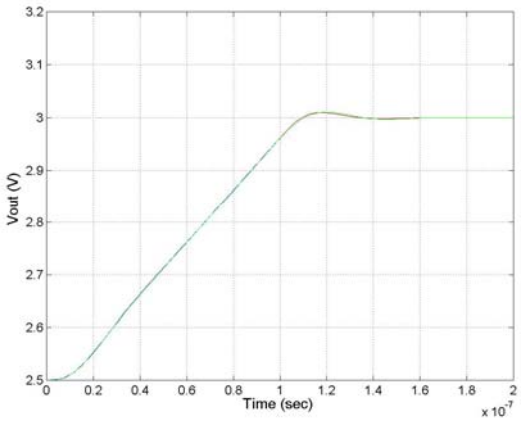
where B_i (i=1, 2, 3) are function of initial conditions that are associated to the time between both time periods, i.e. $t=T_{min}$.

5. RESULTS

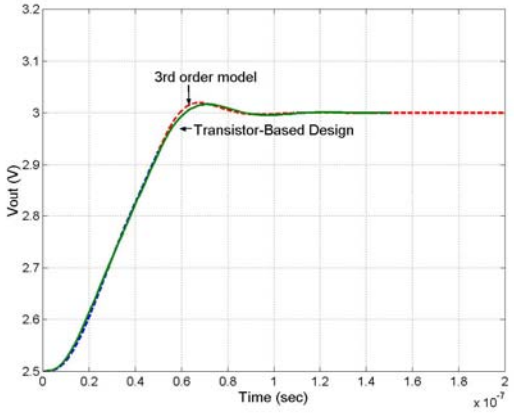
Basic data that define the singularities are σ=-3.5×10^{9}rad/s, α=-7.2×10^{7}rad/s and β=-1.2×10^{8}rad/s, while small-signal parameters of the opamp are given in Table 3. In this design, the current bias of the differential stage is $I_{BIAS,1}$= 284μA, whereas the output stage drives a current $I_{BIAS,2}$= 142μA. Since the 0dB frequency is approximately 10MHz, the rise time of the input voltage (step signal) is of the order of 100ns. Fig. 4a shows a comparison between the proposed third mathematical model and the transistor level spice simulation. It is clear that the mathematical model fits correctly the spice response. Even more, by changing the rise time of the input signal to 50ns, it is easy to verify that the mathetical model's response corresponds to that obtained from simulation, i.e. both curves present the same settling time value. However, a small difference during the slewing period appears in both responses, fortunately even when the third-order mathematical model presents an overshot, it does not affect the whole settling response (see Fig. 4b).

Parameter	Value	Units
g_{mn1}	6.75×10^{-4}	S
g_{mp6}	1.51×10^{-4}	S
g_{ds2}	3.87×10^{-7}	S
g_{ds4}	2.04×10^{-6}	S
g_{ds7}	5.52×10^{-7}	S
g_{ds6}	2.03×10^{-6}	S
C_{db2}	6.88×10^{-23}	F/area
C_{db4}	4.03×10^{-24}	F/area
C_{db7}	0	0
C_{db6}	4.01×10^{-24}	F/area
C_{gs6}	4.45×10^{-14}	F

Table 3. Basic parameters of the Miller opamp for settling analysis



(a)



(b)

Figure 4. Comparison between the third-order mathematical model and the spice response. When the rise time of the input signal is of the order of 100ns or higher, both curves match each other (a); however, for low values of the rise time (for example 50ns), a tiny difference appears between curves(b)

6. CONCLUSIONS

In this paper, basic network analysis was used to propose a third-order transfer function as a suitable design approach to model the time response of the compensated Miller operational amplifier. The amplifier was designed according to design rules of a standard 1.5μm CMOS fabrication process, and simulated with the help of the transistor model (LEVEL=3) given by the manufacturer. Simulation results based on both transistor level design and its lumped equivalent circuit correspond to the response of the third-order model which makes of this proposal a suitable design tool not only for the IC designer, but also for the beginner. The results obtained from this proposal correspond to the best settling model reported up to now [2], [3].

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Authors Biography

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Was born in San Luis Potosí, Mexico. He received the B.E. degree in physics-electronics from the USLP in 1988, Mexico, and the D. Sc. degree in electronics from INAOE, Mexico in 1997. From 1991 to 1996, he worked in the Microelectronics Laboratory at INAOE as a researcher developing wet-etching techniques and designing CMOS circuitry for silicon-based microsensors. In 1997, he was at CNM in Bellaterra (Spain), as a visiting researcher being involved in the development of surface micromachining techniques for developing a fully-integrated microphone. In 1999, he joined CINVESTAV, Guadalajara Unit, Mexico. From 2002 to 2006, he was the coordinator of the Electronic Design Group. His research areas include development of automatic test boards, silicon-based sensors development, low-voltage low-power design circuits, silicon-based DC-DC converters and mixed-mode circuits for both RFID applications and multi-standard communications.

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