# Ring CMOS NOT-based Oscillators: Analysis and Design

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ABSTRACT

This paper presents design hints in CMOS ring oscillators based on NOT gates. The NOT gate is used as vehicle to introduce basics on signal propagation and also to present simple design models. Both simulation and experimental results are presented in order to show the usefulness of the design models. However, for high frequency oscillators several design strategies that are translated at layout level are also described not only to minimize undesirable effects, but also for testing the circuit under study (CUS).

KEY WORDS: Microelectronics; dispositivos semiconductores; field effect integrated circuits.

RESUMEN

Esta publicación presenta recomendaciones de diseño en osciladores de anillo basados en compuertas NOT. La compuerta NOT se usa como medio para introducir fundamentos de propagación de señales y para presentar modelos simples de diseño. Se presentan resultados de simulación y experimentales para mostrar la utilidad de los modelos de diseño. Sin embargo, para aplicaciones de alta frecuencia diversas consideraciones de diseño son incorporadas a nivel layout, no sólo para minimizar efectos no deseados, sino también para caracterizar eléctricamente los circuitos bajo estudio.

PALABRAS CLAVE: Microelectrónica; semiconductor devices; circuitos integrados de efecto de campo.

PACS: 84.40.-e; 85.30.-z; 85.30.Tv

## 1. INTRODUCTION

Due to its simplicity and ease of implementation, ring oscillators (ROs) play an important role in several fields of application. In this paper, useful design hints for designing oscillator circuits based on NOT gates are supported by analyzing the response of the RO in the time domain; ROs have been designed and fabricated by using facilities of standard CMOS technologies. The effect of some non-idealities in the ROs' performance is analyzed as well as proposals for minimizing its anomalous response is also given.

## 2. THE RING OSCILLATOR

In this section, the analysis in the time domain of the NOT gate is presented with a discussion about the design of the NOT-based ring oscillator. The simplest ring oscillator is a closed loop that comprises an odd number of identical NOT gates, forming an unstable negative feedback circuit. The period of oscillation (T) is twice the sum of the gate delays in the ring. The delay ($\tau_d$) of a NOT gate is defined as the time between when the input crosses the toggle point ($\frac{1}{2}V_{DD}$) and when its output crosses the toggle point (see Fig. 1). Another way to calculate the delay is by measuring the average switching time ($\tau_s$) as Fig. 1 shows as well. The difference between both techniques may be estimated by calculating the relative error ($\delta$). According to the simulation data shown in Fig. 1, the relative error is given by

$$\delta = \frac{\tau_d - \tau_s}{\tau_s} = -0.034$$ (1)

or equivalently δ=3.4% [**1**]. Because the input ($V_{in}$) in a practical application is not an ideal step, the input waveform used in this example has been generated with a finite slop.
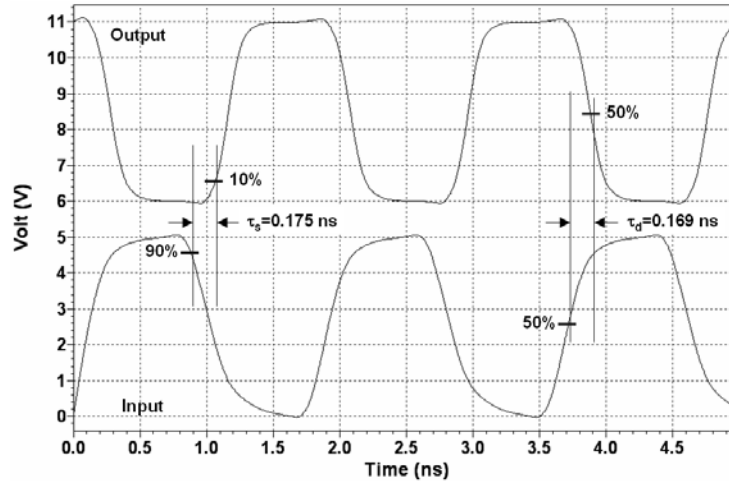


*Figure 1. Spice simulation: propagation delay definition in response to a true voltage input. Here the power supply is $V_{DD}$=5.0 V.*

## A. Design of a RO

The basic circuit is shown in Fig. 2. It is a closed loop comprising N identical NOT gates. One of them - substituted by its equivalent MOS circuit- depicts the nodes of the gate: two nodes for bias purposes ($V_{DD}$ and ground), one node for input the signal $V_{in}$, and another node to measure the response ($V_{out}$). In the same figure, for illustrative purposes, another NOT gate was also substituted by its equivalent layout design. A ring oscillator is designed either empirically or quasi-empirically. The empirical design takes the delay given by the manufacturer, and the right number of stages (N) is chosen in order to obtain the desired frequency. This delay corresponds to the delay of the NOT gate. In practice, the fabrication of a NOT gate produces a parasitic ($C_p$) at the output node affecting the signal propagation. There is also a parasitic at the input node ($C_i$), however, to design a NOT gate the parasitic $C_p$ is the most important due its effect on the NOT gate response.
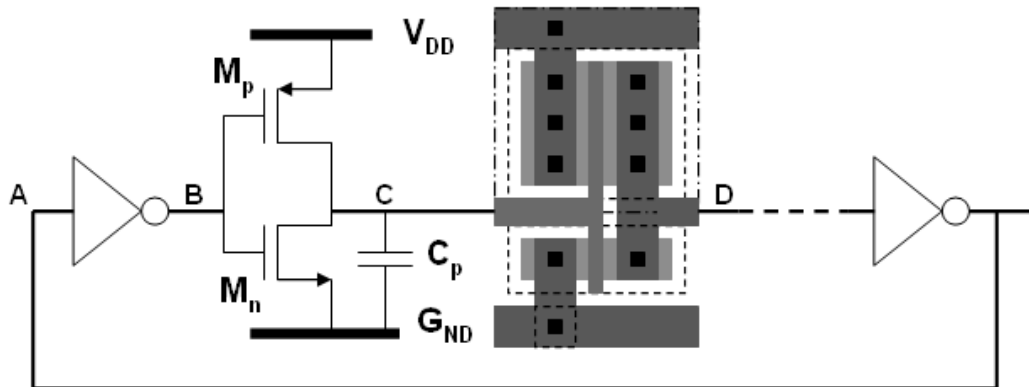


*Figure 2. NOT-based ring oscillator, showing the NOT gate at the transistor- and layout-level.*

Different layout techniques can be applied to minimize the delay in order to increase the oscillation frequency ($f_0$). According to the definition given above, $f_0$ is calculated as follows

$$f_0 = \frac{1}{2N\tau_d}$$

(2)

This result indicates on one hand, that the period of oscillation ($T=1/f_0$) is easily deduced by measuring the oscillation frequency [**2**]. Dividing by the number of stages and by two switching transitions per cycle gives the average switching time, or delay, per NOT gate. This procedure based on a non-complex circuit is simple and used by foundries to measure both the gate delay and the speed-power product. On the other hand, the quasi-empirical method neglects delay data given by the foundry but uses the design ratio ($W_p/W_n$) of the NOT gate to achieve equal noise margin. The design ratio is deduced by using the square-law behavior to model a saturated MOS transistor:

$$I_D = KP_j \left( \frac{W}{L} \right)_j \left( |V_{GS}| - |V_{T,j}| \right)^2$$

(3)

where j defines the transistor type, $V_{T,j}$ is the threshold voltage, and W and L are the width and the channel length of the transistor, respectively. Because the drain current ($I_D$) passes between $V_{DD}$ and ground only when both $M_p$ and $M_n$ are turned on, the following expression is deduced:

$$W_p = W_n \frac{KP_n}{KP_p} \cdot \left( \frac{V_{DD} - 2V_{T,n}}{|-V_{DD}| - 2|V_{T,p}|} \right)^2$$

(4)

where $V_{in}=|V_{GS}|=\frac{1}{2}V_{DD}$ was used. In practice, both design approaches are commonly refined by simulation because of the second order non-idealities neglected by Eq. (3). However, the quasi-empirical approach is the way to design at layout level basic primitives as the NOT gate is. Substituting technological parameters in Eq. (4) the design ratio is within the range

$$3 \leq \frac{W_p}{W_n} \leq 4$$

(5)

where $W_n$ is a parameter under the designer's control. Notice that the oscillation frequency is not under the designer's control. Thus, N is apparently the unique parameter to control $f_0$ as indicated in Eq. (2). Defining $\tau_d \approx R_{eq}C_p$ yields

$$f_0 = \frac{1}{2NR_{eq}C_p}$$

(6)

where $R_{eq}$ is the equivalent resistance at the toggle point. At this point, the NOT gate drives its maximum current ($I_{MAX}$) and Eq. (6) can be written as

$$f_0 = \frac{1}{2NC_p} \cdot \frac{I_{MAX}}{V_{DD}}$$

(7)

In order for Eq. (7) to remain valid, simulations of a three-stage ring oscillator based on a NOT gate was carried out by varying the voltage $V_{DD}$. The oscillator response was input to a NOT gate, and $I_{MAX}$ was obtained as shown in Fig. 3. Simulation results show not only the reduction of the oscillation frequency, but also a non-linear behavior of the rate $I_{MAX}/V_{DD}$. So, as $V_{DD}$ reduces and $I_{MAX}$ becomes lower, $f_0$

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reduces too because $I_{MAX}$ is falling down faster than $V_{DD}$. As an example, Fig. 4 shows experimental result of a 21-stage NOT-based ring oscillator; the effect of $V_{DD}$ on the ring oscillator performance is clearly evident. The CUS was characterized by varying the power supply ($V_{DD}$) in defined steps $\Delta V$=25 mV and measuring the oscillation frequency with the help of a mixed-mode oscilloscope (Agilent, 54622D). The fact that $V_{DD}$ can be longer than 1.0 V has significant implications on low-voltage applications. For example, for a given $f_0$ with minimum variation, $V_{DD}$ can be used as a control voltage by regulating it via a PLL. This fact means that few loop iterations would be needed to shift the frequency to the correct value. That is most notorious in the range 1.0 V$\leq V_{DD} \leq$ 1.25 V. However, for $V_{DD}$>1.25 V it is also possible to shift $f_0$ towards correct values by applying more iterations than before. A voltage-controlled oscillator as described is commonly known as VCO. Notice that, from experimental data shown in Fig. 4, it is possible to know the delay as function of the voltage $V_{DD}$, i.e. for $V_{DD}$=5.0 V a delay $\tau_d$=1.6ns was computed. This result means that a three-stage ring oscillator would oscillate at a frequency $f_0$=104.1 MHz. Therefore, to obtain oscillation frequencies of several hundreds of MHz, facilities of submicrometric CMOS technologies must be used for; alternatively the power supply $V_{DD}$ can be increased but the dynamic power consumption increases too.
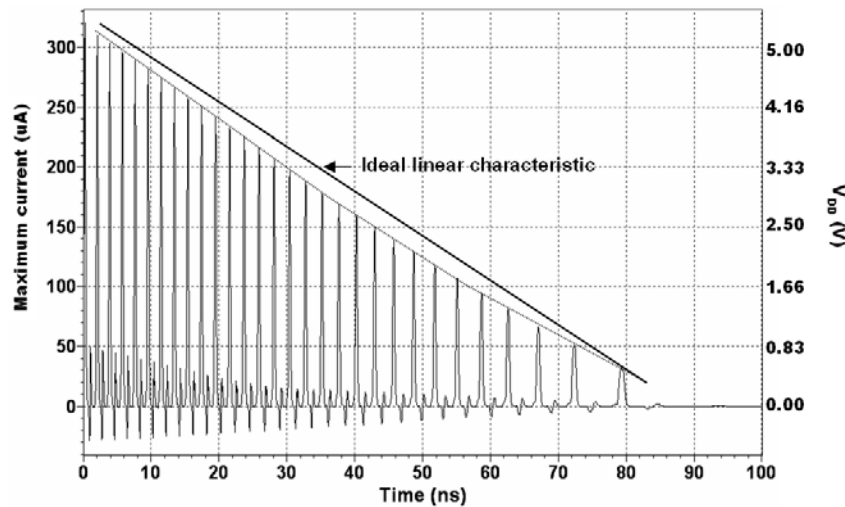


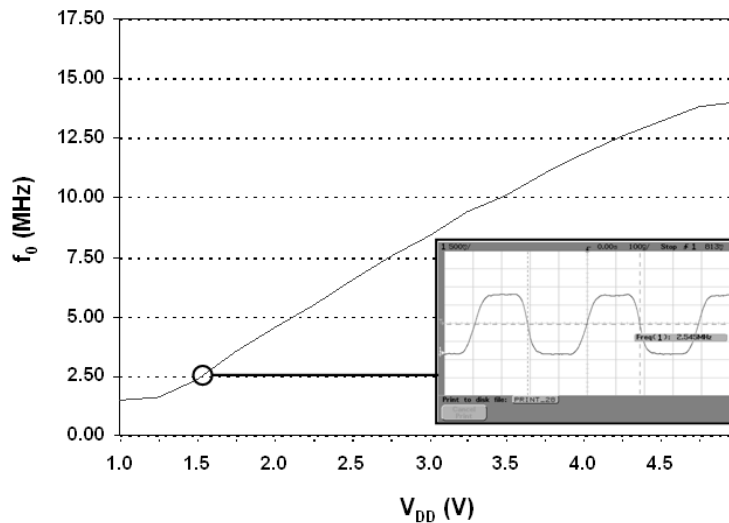*Figure 3. Spice simulation: maximum current driven by the NOT gate as a function of $V_{DD}$.*



*Figure 4. Experimental data: frequency versus voltage for a 21-stage RO. This circuit was fabricated in a*

## B Scaling down the delay

Figure 5 shows the simulation result of a three-stage RO, where the NOT gate was designed according technological design rules of a standard $0.5\mu m$ CMOS process. The aspect ratio, $W_p/W_n = 3$, was obtained with the help of Eq. (4). In order to evaluate the parasitic effect on the RO performance, post layout simulations were carried out by using the LEVEL=49 model for MOS transistors. The oscillation frequency can be lower than 1.12 GHz (see Fig. 5) by increasing the stage number. For example, if **N**=5 the RO produces an oscillation frequency $\mathbf{f_0}$=671 MHz at $\mathbf{V_{DD}}$=5.0 V. That means not only a frequency reduction of approximately 50%, but also a signal with amplitude of 5.0 $\mathbf{V_{pp}}$. Simulated waveform in Fig. 5 shows that the output signal successively exhibits an amplitude lower than 5.0 V; to enhance the waveform, a pair of NOT gates can be series-connected at the output node of the RO.
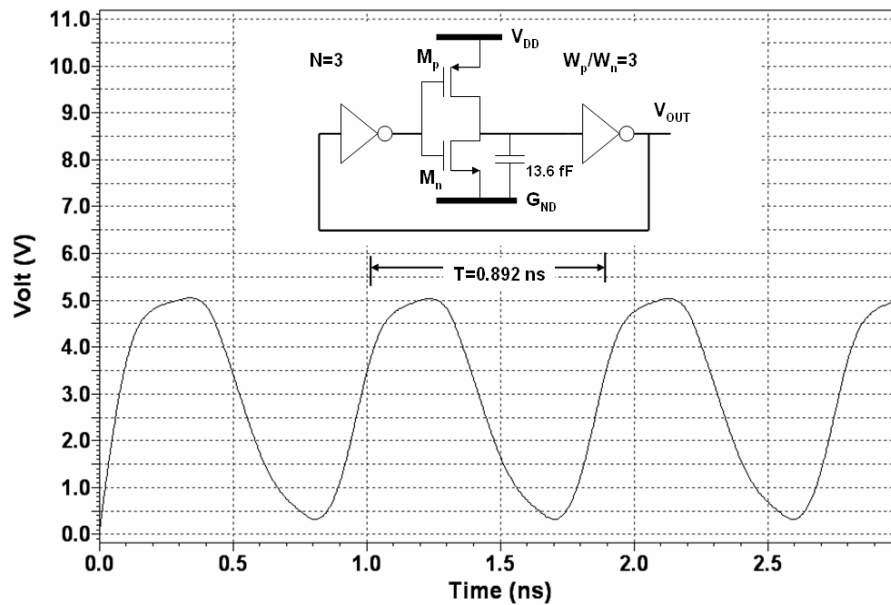


*Figure 5. Spice simulation: the three-stage ring oscillator response for a transistor width Wn=1.5μm.*

In order to explain why the RO presents an oscillation frequency of 1.1 GHz for **N**=3, it is basic to underline that the simulation of the RO does not include a load ($\mathbf{C_L}$) making the simulated waveform an ideal response. In practice, since a RO is commonly embedded in a system, there are digital blocks that process data according to the timing given by the oscillator circuit. Therefore, these blocks present a load $\mathbf{C_L}$ affecting the average switching time. The simulated waveform as a function of the load $\mathbf{C_L}$ is shown in Fig. 6. The fact that $\mathbf{C_L}$ can be higher than $C_p$ represents serious implications on the ring RO applications. On one hand, for a given $\mathbf{C_p}$, as the oscillation frequency requirement increases and $\mathbf{C_L}$ becomes bigger, a capacitive driving circuit is needed to drive large capacitances. Otherwise, the waveform goes beyond the expected one as the Fig. 6 shows. On the other hand, by adding a driving circuit (buffer) the total power consumption of the whole design increases.
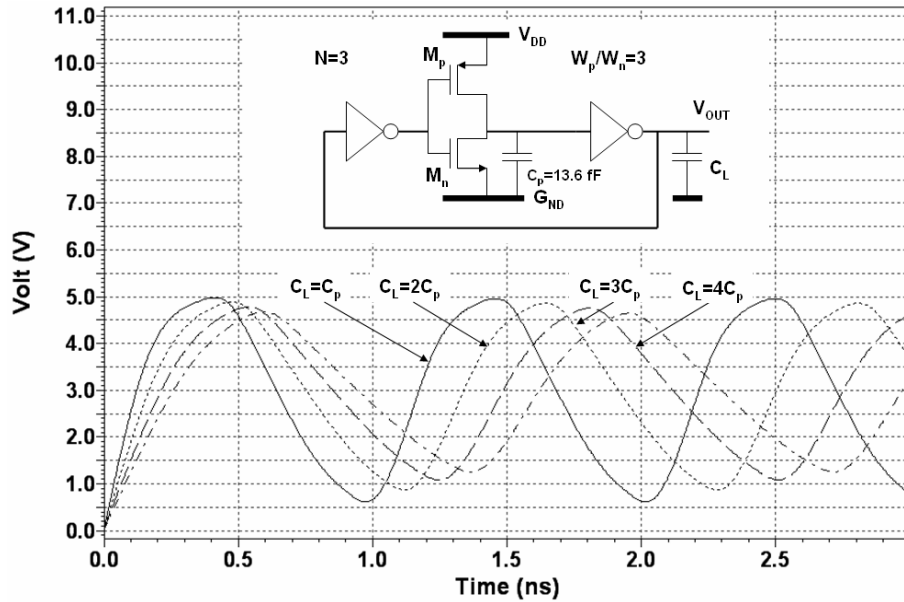
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*Figure 6. Spice simulation: ring oscillator response as a function of the capacitive load.*

Figure 7 shows experimental results of the 21-stage RO presented in Fig. 4, where measurements were carried out without a buffer; the same figure also shows the IC under analysis. Since the effect of parasitics affect the charge/discharge time, the amplitude of the signal is lower than the magnitude of power supply $V_{DD}$=5.0 V. Therefore, the buffer design must be done in order to eliminate the effect of parasitics on the RO performance. On the other hand, a design hint for designing an IC for academic/research purposes (also called test chip) is saving the PADs number. Saving PADs means not only minimizing parasitics, but also saving both integration area and power consumption. For instance, to validate simulation results of ROs (**N**=3, 5, …) the test chip must include a couple of PADs to power all oscillators, a unique PAD to measure the response of the oscillators, and consequently just one buffer to drive the whole load capacitance. This design strategy demands an **m**:1 digital multiplexer, where **m** is the number of ROs to be tested. However, if test facilities include on-wafer equipment for radio-frequency (RF) measurements, buffer, multiplexer, and the package can be avoided. Any else, the early strategy is the correct one but high frequency effect must be taken into account in order to test mainly ROs for RF applications.
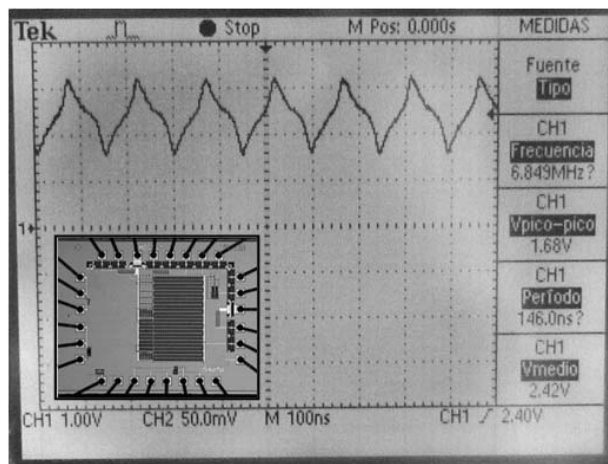


*Figure 7. Experimental data: unexpected response due to the effects of a high capacitive load*

## 3. HIGH FREQUENCY EFFECTS

In this section, the analysis of radio frequency (RF) effects are presented with the help of useful math models. One of these RF effects is that associated with the frequency-depended resistance on wires commonly know as the skin effect. This name is due to the tendency of an AC current to distribute itself within a wire [**1**]. For instance, for DC applications the resistance of a wire is given by

$$R_{DC} = \frac{l_w}{\pi a^2 \sigma} \qquad (8)$$

where $l_w$, **a**, and $\sigma$ are the length, radius, and conductivity of the wire, respectively. However, in the frequency domain the wire resistance follows

$$R_{AC} = R_{DC} \frac{a}{2\delta} \qquad (9)$$

with $\delta$ the so-called skin depth commonly modeled by

$$\delta = \sqrt{\frac{2}{\mu_0 \sigma \omega}} \qquad (10)$$

where $[\omega]$=rad/s, $[\delta]$=m, and $\mu_0$=1.2566×10$^{-6}$mkgC$^{-2}$. Fig. 8 shows the skin depth response in the frequency domain where the conductivity of copper ($\sigma_{Cu}$=58×10$^6$ $\Omega^{-1}$m$^{-1}$) was used for illustrative purposes. The meaning of the response is that, as the frequency of the signal increases, the density current near the surface of the wire is greater than that of its core or, in other words, the AC resistance of the wire increases. The same tendency is found with other conductive material as silver ($\sigma_{Ag}$=63×10$^6$ $\Omega^{-1}$m$^{-1}$), aluminum ($\sigma_{Al}$=37×10$^6$ $\Omega^{-1}$m$^{-1}$), or gold ($\sigma_{Au}$=45×10$^6$ $\Omega^{-1}$m$^{-1}$). On the other hand, the layout of the three-stage ring oscillator shown in the Fig. 5 includes an aluminum-based feedback bus having a length $\ell$=19.2μm, whereas the length of the bus for **N**=5, 7, and 9 corresponds to 31.8μm, 43.8μm, and 57μm, respectively. In order for Eq. (9) to remain valid, it is well known that the area of a rectangular cross-section is equivalent to a circular one by defining the radius **a** as follows

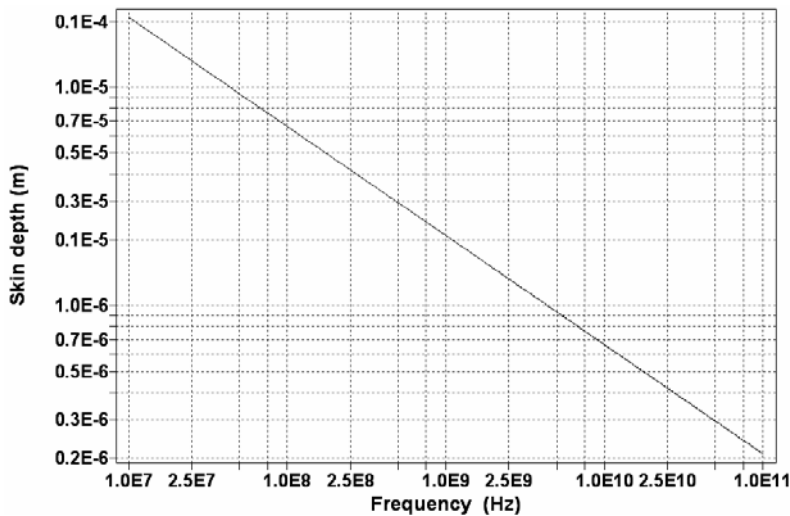$$a = \sqrt{\frac{W_{bus} h}{\pi}} \qquad (11)$$



*Figure 8. Spice result:* δ-f *characteristic.*

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where **W**$_{bus}$ and **h** are the width and thickness of the bus, respectively. Fig. 9 shows the AC resistance of the aluminum-based bus in the frequency domain as well as the oscillation frequency generated by each RO according to its corresponding bus length.
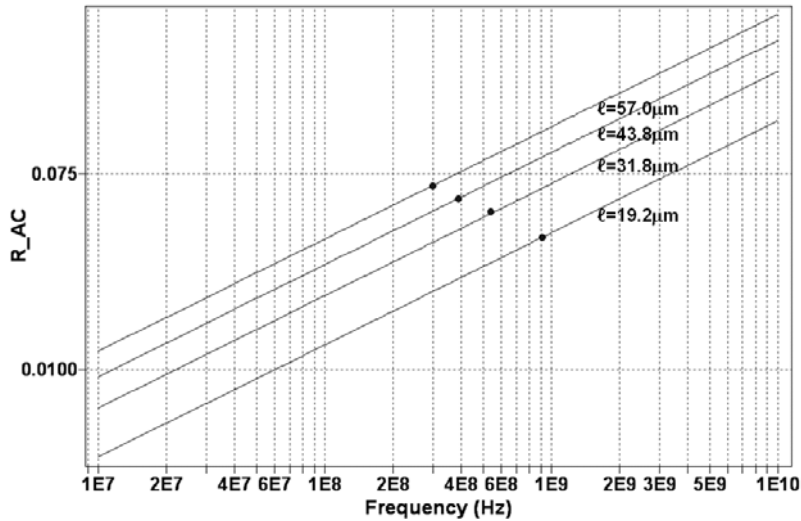


*Figure 9.Spice result:* $R_{AC}$-f *characteristic, where* $[R_{AC}]=\Omega$ *and* $W_{bus}=1.2\mu m.$.

Another RF effect is that of the parasitic inductance effect due to conductors. Taking into account both design parameters and technological data for the aluminum-based bus analyzed above, it is simple to estimate the self-inductance of the bus with the help of the following model [**2**]:

$$L_{ms} = 2\ell\left[ \ln\frac{2\ell}{W_{bus}+h} + \frac{1}{2} + \frac{W_{bus}+h}{3} \right]$$ (12)

where h=700 nm [**3**]. Table 1 summarizes computed parameters of the RO for each stage number. Since the oscillation frequency is lower than 1.0GHz, the total impedance of the feedback bus is purely resistive. Therefore, for the purpose of this design, parasitic effects do not alter the performance of the RO (see Fig. 10).
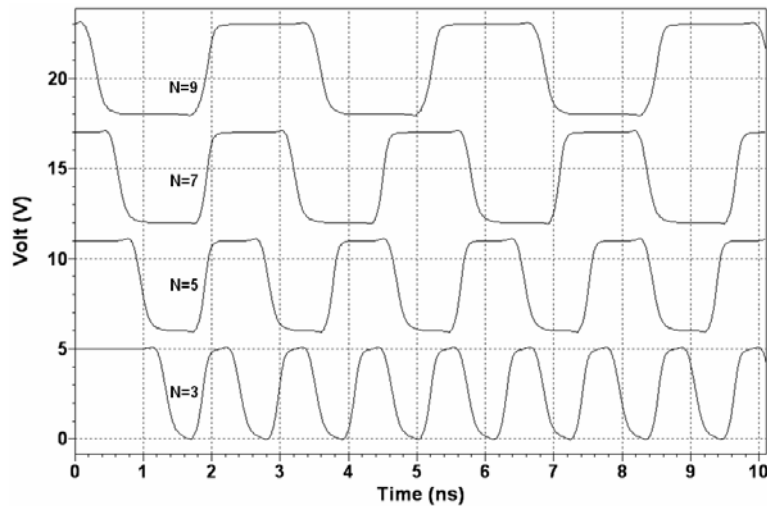


*Figure 10. Spice simulation: Unwanted RF effects do not alter the response of the RO.*

## 4. THE TEST PROCEDURE

In this section, design considerations for designing a test chip are presented with a discussion of suitable test procedures. In order to save integration area, a digital 4:1 multiplexer can be also integrated in conjunction with few ÷2 circuits. Because a signal with a frequency of $\frac{1}{2}f_0$ can be obtained from $f_0$ by frequency dividing, at least four ÷2 circuits are needed to obtain a signal with a frequency lower than 100MHz. That is true when test facilities are limited up to 100MHz measurements. In other words, not only integration area savings dictate the design of a test chip, but also the development of test strategies. Alternatively, a lower integration area is needed by designing a unique ÷4 circuit. That fact does not modify the test strategy. The latest is mainly supported by the access to test facilities as Fig. 11 shows. The same figure shows that just one output pad in needed to measure the response of the ROs via an oscilloscope. However, to drive the whole load capacitance one buffer based on NOT gates may be added as part of the test strategy [**4**]. On the other hand, in this example the layout of the ROs occupy an area of $69\times39\mu m^2$ that corresponds approximately to four times the cross section area of the average human hair. In practice, the layout design of the whole circuitry must be compact and preferably based on a regular shape as Fig. 7 shows. The latest diminishes unwanted effects and guarantees that the experimental response corresponds to that deduced from spice simulations. Alternatively, it is recommended that the test chip includes basic primitives for individual characterization. MOS transistors, gates, buffers, switches, and some passive components are examples of them. Furthermore, for testing purposes, each primitive must include its own pads in order to avoid the effect of its operation on the performance of other primitives. Any else additional cautions at layout level have to be taken in account. At the end, the purpose is successfully verifying the basic operation of the primitive under test. The advantage of testing primitives is that the designer uses technological data for enhancing design models and also to fit design parameters.
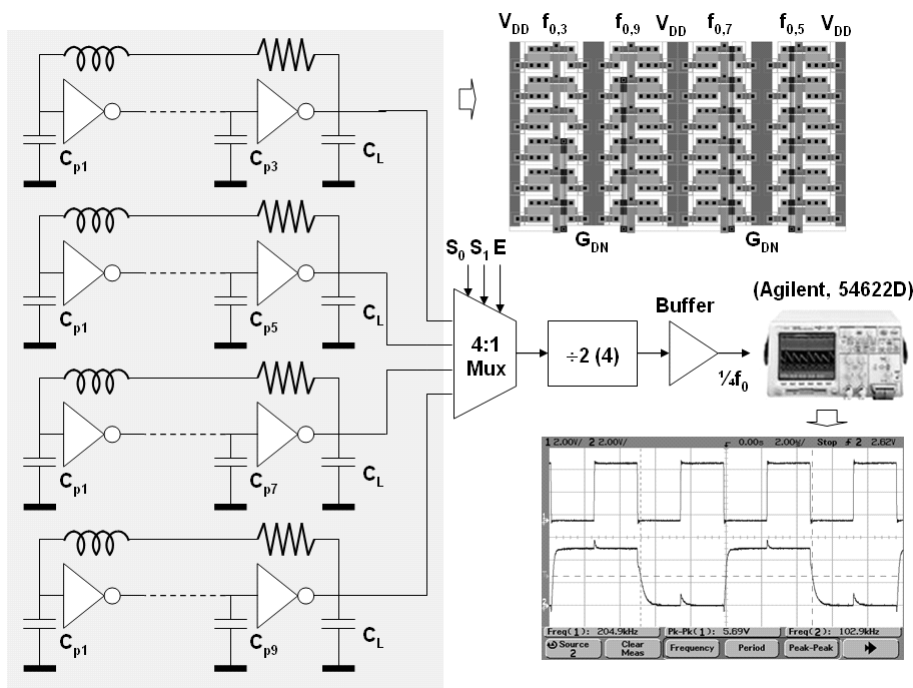


*Figure 11.Test strategy based on one output node for measuring a set of four ROs.*

## 5. CONCLUSION

Design issues for designing CMOS ring oscillators based on NOT gates have been presented. The NOT gate and its average switching time have been used to introduce not only basics on signal propagation,

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but also to diminish unwanted effects mainly for high frequency applications. In order to illustrate the design hints based on simple math models, both simulation and experimental results have been presented. However, since output pads as well as silicon area must be optimized, a test procedure based on a single output pad was presented also as a vehicle to introduce other basic blocks of which multiplexers, frequency dividers, and buffers are just some examples. The test procedure is simple and also suitable for using basic lab equipment. Finally, for training purposes, IC design tools can be downloaded from the link www.tanner.com .

## 6. ACKNOWLEDGMENT

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