AN AUTOMATIC TEST ENVIRONMENT FOR MICROELECTRONICS EDUCATION AND RESEARCH

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ABSTRACT

An automatic test environment (ATE) based on a PSoC has been developed to perform electrical characterization of integrated circuits (ICs). The ICs are designed for academic and research purposes as part of the Electronic Design graduate program at CINVESTAV-Guadalajara Unit; these ICs are manufactured in standard N-well, 5-V, 1.5μm/0.5μm CMOS technologies. The ATE offers programmable capabilities to develop master-slave architectures, memory for data storage, functions generator to stimulate circuits and systems, current/voltage sources for several purposes, current-voltage measurements, and ports to download experimental data to a PC. To date, several ICs have been tested with the help of the ATE. In this paper, however, examples based on MOS Transistors only are presented in order to describe the ATE performance and also to show how experimental data of the devices under characterization were validated through SPICE simulations, experimental data given by manufacturers, and using commercial equipment as well.

KEY WORDS**:** Microelectronics, electric variables measurement, teaching.

RESUMEN

Se ha desarrollado un *ambiente automático de pruebas* (ATE) basado en un PSoC comercial para realizar la caracterización eléctrica de circuitos integrados (CIs). Los CIs son diseñados para propósitos académicos y de investigación como parte del programa de posgrado de la Unidad Guadalajara del CINVESTAV; esos CIs son fabricados en tecnologías pozo-N, 5-V, 1.5μm/0.5μm CMOS estándar. El ATE ofrece capacidades de programación para desarrollar arquitecturas *amo-esclavo*, memoria para almacenar información, generador de funciones para estimular circuitos y sistemas, fuente de voltaje/corriente para diversos propósitos, mediciones en voltaje/corriente, y puertos para descargar información experimental a una computadora personal. A la fecha, varios CIs han sido caracterizados con ayuda del ATE. En esta contribución, por cuestiones de espacio, se presentan algunos ejemplos basados en transistores MOS para mostrar la operación del ATE y también para mostrar cómo los resultados experimentales de los dispositivos bajo caracterización se validaron a través de simulaciones SPICE, de información experimental dada por los fabricantes, y también usando equipo de medición comercial.

PALABRAS CLAVE: Microelectrónica, medición de variables eléctricas, enseñanza.

1. INTRODUCTION

The aim of the project is to develop an automatic test environment (ATE) that enables the electrical characterization of integrated circuits (ICs) for microelectronics education and research. Such development is, at the same time, the author's solution to face the need of test equipment. The proposed ATE is a versatile test hardware focused to perform not only electrical characterization of circuits and systems, but also to develop test strategies by using either software or firmware. In practice, while an

ATE for industrial purposes (IPs) may be oriented to perform the whole evaluation of a new product, academic areas may require an ATE to mainly verify the functionality of the ICs designed by their staff. The ATE for IPs is expensive and involves personnel with skills to evaluate experimental results according to both international standards and industrial quality indices. An ATE for academic purposes, on the other hand, may be expensive or not depending of academic test requirements. Ideally, laboratory work in microelectronics should be a time for students/researchers to experience/evaluate the complexities of real silicon-based ICs by integrating many of the topics they have learned/proposed in courses/research projects. Unfortunately, working with the ICs designed for academic/research purposes is difficult in a breadboard-based graduate laboratory, where the ICs designed by the staff are packaged in either LCC28 or LCC52 units. Further, difficulties of laboratory work increase when basic equipment[1] is not enough (or it does not exist) to perform basic electrical characterization of devices, circuits, and systems.

How can an electronic design laboratory face the electrical test of ICs so that the experience not only is exciting and motivating to the students, but also is supporting the growing of the staff's research? This is the question that has driven the development of a PSoC-based automatic test environment at CINVESTAV-Guadalajara Unit. Currently, there is no report about the development of an ATE for both academic and research purposes except one work that describes basic circuits based on commercial components to also face the need of test equipment [1]; other works underline the need of custom developments supported in both commercial components and test equipment [2]-[6].

2. ATE DESING

In this section, the PSoC-based ATE is presented with a discussion of related technical issues. In general, this development is a portable test board that includes the following characteristics: 1) programmability to develop master-slave architectures, 2) memory for data storage, 3) functions generator to input either current- or voltage-based signals to devices, circuits and systems, 4) current/voltage sources for bias purposes, and 5) ports to download experimental data to a PC. Furthermore, this development satisfies technical and economical specifications including eight/four digital/analog channels, mixed-signal capabilities, +5V/-5V/±12V operation at 130mA/55mA/30mA, 0-5V/0-5V input/output range voltage, at least one output current port, programmable output current range, minimum number of commercial components, reduced PCB size, and low-cost. Fig. 1 shows the 10.0×12.5 cm^2 test board designed in a FR-4 substrate and integrating four active layers (two/two planes for ground/signal). Since the device under test (DUT), liquid crystal display (LCD in Fig. 2), and PC are external entities to the test board, they have been omitted in this figure.

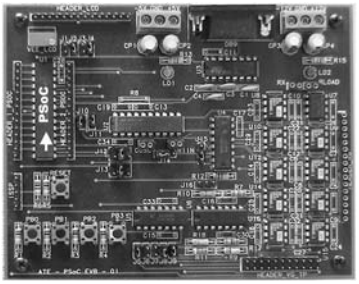

Figure 1. Demonstration of the evaluation board or ATE. The arrow indicates where the PSoC is; other components are external resources including connectors for PC/LCD communication, push bottom-based keyword, and power supply.

[1] Basic test equipment refers to AC/DC current/voltage sources, function generators, and multimeters.

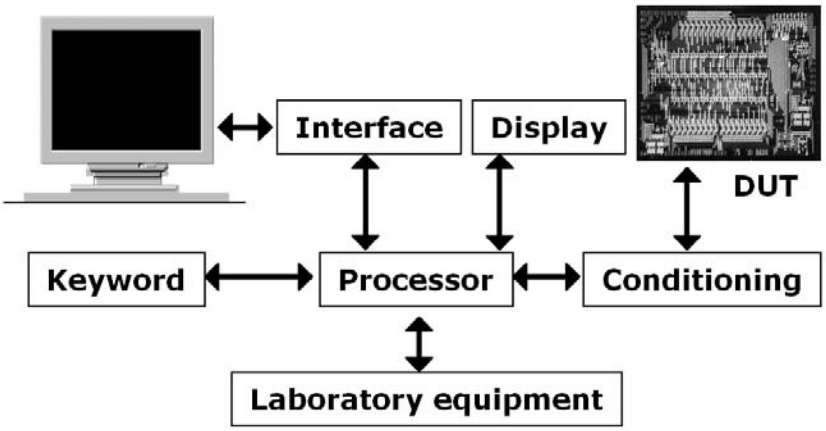

Figure 2. Diagram block of the network-based ATE.

The ATE architecture exploits paradigms of multipurpose operations like those inspired by networks, i.e. the decision area in control of both internal and external peripherals is the *Processor* block shown in Fig. 2. The processor is actually a commercial PSoC, whereas the *Conditioning* block represents external peripherals needed to generate/measure input/output signals among other capabilities. In this case, the ATE provides quality results by maximizing not only the operation of all resources, but also by optimizing communication protocols between them [7].

Since the PSoC is a 24MHz mixed-signal processor with reconfigurable capabilities, it was chosen over other processors (based on fixed architecture) because, adding other components, the PSoC-based ATE offered the lowest cost. Omitting the cost of the PC, the investment of the ATE (one test board) is approximately of 75 usd.

On the other hand, and taking into account the basic test needs mentioned early, to perform analog and digital characterization tasks, the PSoC-based ATE certainly requires few external peripherals because, for this development, the PSoC's resources (also called internal peripherals) are configured according to characterization needs.

Few external peripherals represent a small PCB which makes the ATE a low-cost portable development. From the point of view of programmability, the PSoC gives the electronic design staff the opportunity to take advantage of all peripherals embedded in the PSoC, including analog-to-digital (A/D) and digital-to-analog (D/A) converters, memory access, and one timer. The CY8C29466 device, the author's choice, is a 24 MHz PSoC. For example, this device can be configured to obtain resolutions of A/D converters from 6- to 14-b, as well as from 6- to 9-b for D/A converters [8]. D/A converters are used to build up to four incremental voltage sources whereas just one 12-b A/D converter is required to measure up to eight voltage variables.

The latter is performed by adding an analog multiplexer (CD74HC4051, TI) [9]. In addition to that, it is possible to measure those voltage variables with the help of lab equipment[2] (*Laboratory equipment* block in Fig. 2) by developing master-slave architectures. The communication between the PSoC and external peripherals is based on serial port pins under the standard EIA/TIA-232, where the ST232CN device was added to acquire experimental data [10].

The ATE communicates with the PC via a serial receiver/transmitter (8-b TX8/RX8). In order to control the data rate, the counter of the PSoC was configured at 9600 bauds.

[2] In this paper lab equipment refers digital oscilloscopes, impedance analyzers, and spectrum analyzers.

3. FUNCTIONS DESCRIPTION

In this section, several functions for exploiting the ATE capabilities are presented with a discussion of practical examples. Experimental data are obtained by running several functions that configures some PSoC peripherals according to well-established architectures. Some of these functions are the following:

CS - Defines a current source
VM - Performs voltage measurements
VF - Calls a frequency measurement
VS - Defines a voltage source
IM - Performs current measurements
DD - Downloads data to a PC

As it shall be described, currently the ATE development does not include a programmable resistor array needed to measure electrical current or equivalently to define current ranges measurement. Alternatively, when current measurements are needed an external resistor is added to the ATE. The nominal value of this resistor is neglected, and the resistance measurement is achieved with help of two functions: **CS** and **VM**. By running **CS**, the current source depicted in Fig. 6 is defined, where AD620 and TL081 are external peripherals. Note that the current I_x is actually obtained from the voltage-controlled current-source definition, i.e. the magnitude of the current source is obtained by measuring the voltage V_{set} and then using the relation $I_x=V_{set}/R_x$, where R_x is a known value. Next, when this current flows through the LOAD a DC voltage measurement (V_{LOAD}) is achieved by running the function **VM**. In practice, LOAD represents a device that obeys the Ohm's low, i.e. passive resistors or diode-connected MOS transistors.

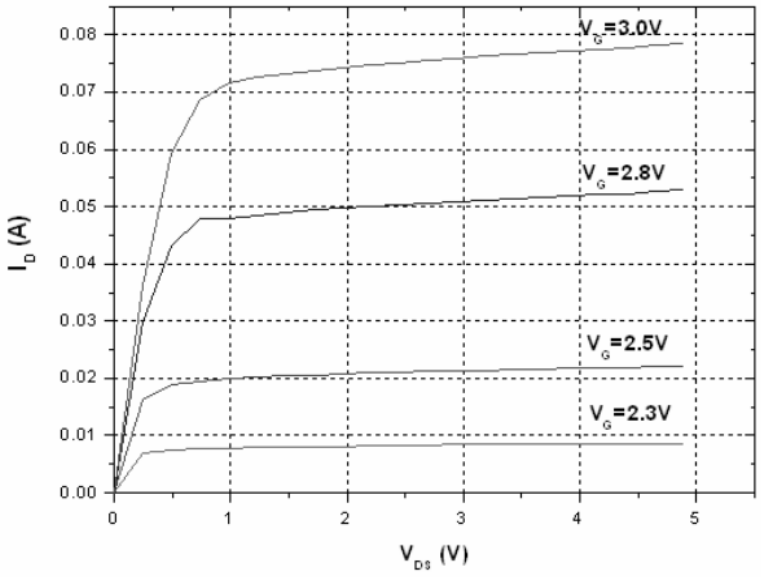

Figure 3 The ATE-based current-voltage characteristic of the 2N7000 transistor corresponds to that reported by the manufacturer.

The voltage-controlled current source presents two basic characteristics: the default value of the step width is t_s=200μs, while the step magnitude can be selected by the user. Once the resistance of LOAD is known, it is connected to DUT to run test steps; some of these DUTs are MOS transistors (N- and P-type), single-ended amplifiers, ring oscillators, voltage dividers based on either passive resistors or MOS transistors, etc. Experimental data are stored in an output listing format that makes it easy to download them from memory to a PC by running the function **DD** for later analysis.

In Table I the resistance of some commercial resistors (5% tolerance range) is shown. From left to right the nominal value, the value deduced from ATE measurements, and that measured with help of an impedance analyzer (4192A, Agilent) are presented. Note that with the help of both V_{LOAD} and I_x the resistance of these resistors is obtained by applying suitable data analysis once experimental values were downloaded to a PC; the ATE does not include a numerical processor. On the other hand, defining $X_{(M)}$ and $X_{(N)}$ as measured and nominal values, respectively, the classical way for expressing accuracy is as follows:

$$\Delta_{(X)}=X_{(M)}-X_{(N)} \quad (1)$$

$$\delta_{(X)}=\Delta_{(X)} / X_{(N)} \quad (2)$$

where (1) and (2) are the absolute and relative error, respectively. Table I illustrates also the error deduced between the nominal value and both the Impedance analyzer (IA) and the ATE; the error is given in the format $\delta_{(X),IA}/\delta_{(X),ATE}$. As Table I shows, the IA produces lower errors than the ATE measurements; the difference is due to the offset of the converters embedded in the ATE. Thus, to obtain equivalent errors to those of the IA, the voltage-controlled current-source has been programmed to supply a current I_X >0.72 mA. This example has a twofold purpose: 1) the IA was used as a reference tool to compare values obtained with the help of the ATE, 2) the characterization of resistors allows establishing the operation range of the **CS** in order to obtain true experimental values.

Manufacturer (Ω)	Agilent 4192A (Ω)	ATE (Ω)	Error (%)
1.2k	1.211k	1.217k	0.90 / 1.39
1.5k	1.467k	1.477k	2.24 / 1.55
1.8k	1.803k	1.817k	0.16 / 0.93
2.0k	1.999k	1.982k	0.05 / 0.90
2.2k	2.203k	2.223k	0.13 / 1.03
2.7k	2.622	2.650	2.97 / 1.88

Table 1. Resistive data comparison

4. ATE ASSESSMENT

In this section, the assessment of some of the ATE's functions is presented with a discussion about why some external peripherals were also added to this development. External peripherals are result of evaluating the electrical characterization of both commercial MOS transistors and integrated MOS transistors.

A. Commercial MOS transistors

The 2N7000 transistor is one of several commercial devices used to design MOS-based circuits for academic purposes. For several years, this transistor has been used in graduate courses[3] as vehicle not only to experience the role of the threshold voltage in the design of active voltage dividers and amplifier stages, but also to obtain its current-voltage characteristic via experimental data [11].

[3] Analog Circuits Design: Part I and II

The advantage of using this component in the ATE assessment is twofold: 1) it allows tuning external peripherals in order to determine the lowest/highest current drain to be measured. The drain current (I_D) is calculated by measuring the voltage drop in a resistor, while the resistor's value is obtained from its current-voltage characteristic according the process described above. 2) With the help of the transistor's data sheet, it is easy to verify that it delivers a high drain current (up to 80mA for V_{GS}<3V) making it necessary to include other peripherals in order to translate that current in a measurable one. It is important to underline that even when the main use of the ATE is oriented to test CMOS-based low-voltage low-power ICs because of the internal projects, the ATE has been designed to also satisfy other requirements as high current measurements.

In order to reproduce the manufacturer data, an external component R_{SHUNT} (≈1Ω) was used to measure the drain-to-source voltage (V_{DS}), and the drain current is calculated from V_{DS}/R_{SHUNT}. Based on this procedure, just one of the A/D converters embedded in the PSoC is configured to 12-b for obtaining the current-voltage characteristic. However, since this converter presents a resolution of 1.22mV and voltages lower than that must be measured, an instrumentation amplifier (AD620) was added to the ATE. Fig. 3 shows the transistor's current-voltage characteristic where upper curves (3- and 2.8-V) correspond to a gain **A**=50, whereas a gain **A**=106 was programmed to obtain the curves for V_{GS}=2.5- and 2.3-V.

Based on the knowledge of the manufacture's data, note that these gain factors were fitted not only to reproduce the transistor's current-voltage characteristic, but also to obtain an error lower than 1%; the error is currently measured in few points of the current-voltage characteristic. On the other hand, it is clear that this transistor is and shall be part of the mentioned curses. Any else a programmable gain factor should be designed and added to the ATE in order to select current ranges as multimeters work.

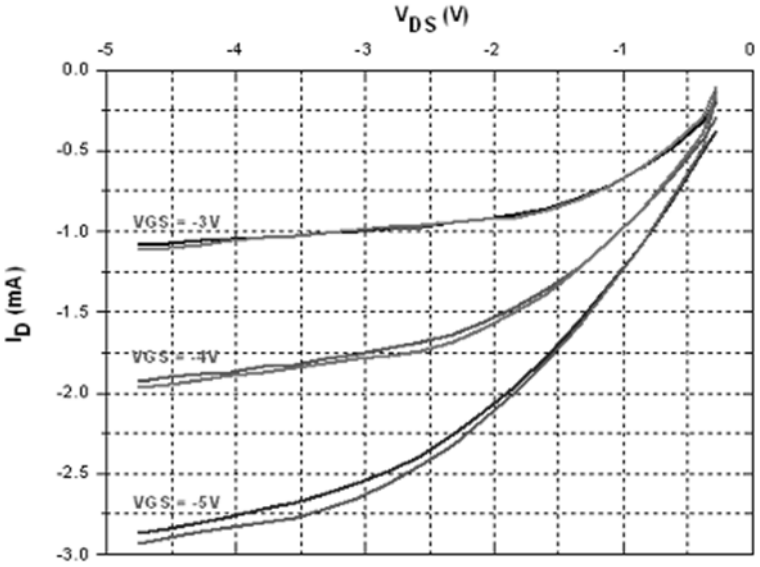

Figure 4 PMOS transistor I_D-V_{DS} characteristic for several V_{GS}. For each pair of curves the upper/bottom one is due to SPICE results/experimental data. The aspect ratio of this transistor is W/L=42μm/1.8μm that is higher than the minimum size allowed by the technology (0.5μm CMOS).

The current voltage-characteristic allows the students to visualize clearly basic operation regions of the transistor: linear and saturation. The effect of the gate-to-source voltage (V_{GS}) on the current I_D is verified as well as the control on the voltage V_{DS} to establish the transistor operation as a voltage-depended quasi-linear resistor (linear region) or as an equivalent current source (saturation region). In practice, it is basic to know all about current and voltage characteristics of the circuit or system under analysis in order to configure the ATE resources (or other test facilities) according to test needs. Once the setup is defined, no more than one minute is required to run voltage sources, process and capture experimental

values, download data, and visualize graphically the I_D-V_{DS} characteristics as function of V_{GS}. This process means that internal/external resources communicate each other in a correct way. However, as Fig. **4** shows, at this point the ATE is unpractical for measuring currents lower than 5mA.

B. PMOS transistor

A low current case study is the room-temperature I_D-V_{DS} characteristic of an integrated PMOS transistor shown in Fig. **4**, where V_{GS}>2V. This transistor was designed according to design rules of a 1.5μm CMOS technology; this transistor as well as other CMOS circuits form a test chip packaged in a LCC28 unit. The I_D-V_{DS} characteristic was obtained with help of a resistor $R_{P\text{-}SHUNT}$=10Ω. The figure shows also a comparison between simulation results and experimental data. In this case, simulation results correspond to an equivalent foundry's data sheet, which is useful to compare simulation results with experimental data and also to estimate measurement errors. The maximum relative error between simulation and experimental curves, at the same gate-to-source voltage, is approximately **3**%.

From the point of view of laboratory, the unique reference data that students have in order to describe and/or explain the current-voltage characteristic of MOS transistors is that of SPICE simulation. The latest is true mainly when the device is tested for the first time. After that, simulation results are substituted by experimental curves (or academic data sheet) because a test chip is fabricated and tested periodically. On the other hand, SPICE is a general purpose circuits simulation software with emphasis in silicon-based ICs; an evaluation version of T-SPICE can be downloaded by following the directions given in [12]. For precision modeling of ICs, the LEVEL=49 model takes into account not only the variation of model parameters as a function of sensitivity of the geometric parameters, but also applies the charge conservation law for precision modeling of MOS capacitor effects. This model, that is given by the foundry, is used at CINVESTAV-Guadalajara Unit for SPICE simulation via T-SPICE. As part of the laboratory activity, on the other hand, students validate their design through simulations and experimental measurements. Next, due to the low drain current driven by the PMOS transistor (see Fig. **4**), students conclude that the identification of the limit between linear and saturation regions is not an easy task. So, for personnel with knowledge on design of electronic circuits, surely the analysis of the I_D-V_{DS} characteristic is a common practice. For students, however, the laboratory experience offers them a motivation to do electronic design mainly when they design and test their own devices. At this point, the author invites the reader to propose a setup for obtaining the I_D-V_{DS} characteristic of a PMOS transistor considering that the measurement process is a voltage-mode approach, i.e. no current measurements must be done.

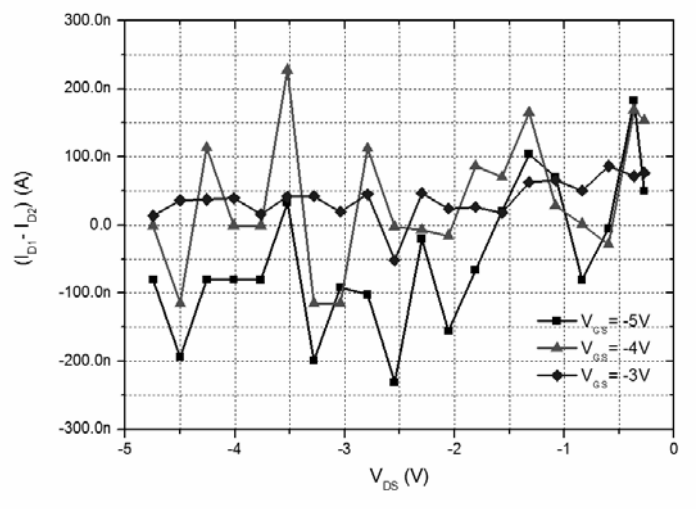

Figure 5. Static current ΔI as function of V_{DS}.

C. Split-drain PMOS Transistor

A research case study is the so-called MAGFET. This device was also fabricated in the same 1.5μm CMOS technology. The MAGFET, used for detecting a magnetic field **B**, is actually a MOS transistor with two adjacent drain regions (D_1 and D_2) which share the drain current I_D ($=I_{D1}+I_{D2}$). In practice, a magnetic field perpendicular to the transistor's channel causes a deflection of the charge carriers in the channel region. The current deflection eventually leads to an asymmetry in the drain current that is an indirect measure of the magnetic field strength. The current asymmetry or current imbalance (i_B) can be estimated by applying differential techniques. The main advantage of differential techniques is that common mode (CM) signals are eliminated. Some CM signals are those due to extrinsic/intrinsic noise sources that affect the measurement of i_B. That measurement is critical when the inversion channel has minimum size. Nevertheless, by increasing the area of the inversion channel, unwanted current contributions are minimized, and the current imbalance would be considered as a noiseless variable. In the 1.5μm CMOS technology minimum size represents an area as small as 1.5μm×3.0μm. Fig. **5** shows the current I_{D1}-I_{D2} for three different V_{GS} voltages with each drain connected to an external resistor (R_{SHUNT}). These room-temperature curves were obtained at **B**=0 by following the test procedure described in Section A. Notice how the three curves change over the V_{DS} axes. The curve due to the voltage V_{GS}= -5.0 V rises from -120 nA and reaches its pick (225 nA) at a voltage V_{DS}= -3.5 V. The curve for V_{GS}= -3.0 V, on the other hand, presents the lowest error (≈ 0.27 %) over the V_{DS} axes. The error, which is measured with the origin at ΔI=0, does not reach the zero requirement but at some voltages, from which the voltage V_{DS}= -2.75 V is one of them. A conclusion at this point is the important role of the voltage V_{GS} for measuring a magnetic field. For example, at the defined operation point, the split-drain MOS transistor drives a whole drain current with a magnitude of 40 μA at both V_{GS}= -3.0 V and **B**=0 [**13**]. Then, the relative error is calculated by

$$\delta_{(I)} = \frac{I_{D1} - I_{D2}}{I_D} \approx \frac{41.6nA}{40\mu A} \equiv 0.10\% \qquad (3)$$

From this result, it is assumed that if the gate-to-source voltage varies in the range -3.25V<V_{GS}<-2.75V, I_{D1}-I_{D2} presents an average value of (50nA+25nA+50nA)/3≈41.6nA (see Fig. **5**). Therefore, unwanted current contributions would be a zero contribution variable if the current imbalance satisfies the condition i_B>4$\delta_{(I)}$. This value not only defines the magnetic field magnitude to be detected, but also is an option to establish the minimum distance between the transducer and the magnetic source.

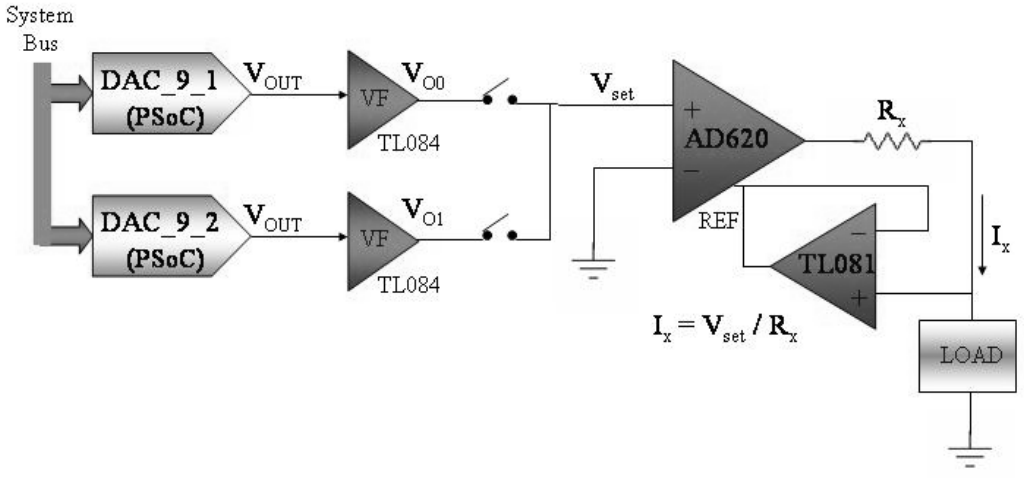

Figure 6. Current source architecture, where LOAD is the component under test.

From the poin of view of the ATE, note that it offers two options for computing current I_{D1}-I_{D2}: 1) by saving the voltage measurements of each drain in memory, download data to a PC and using suitable software, current I_{D1}-I_{D2} is estimated (note that R_{SHUNT} is a known value) ; 2) by using a differential amplifier and knowing the value of both R_{SHUNT} and gain factor, current I_{D1}-I_{D2} is then obtained once data in memory is also downloaded to a PC for process them. Both procedures do not modify the error given in (3).

5. CONCLUSIONS

Taking into account that academic institutions apply different strategies to verify the functionality of the ICs designed by their personnel, in this paper the test process applied by the Design Group at Guadalajara-Unit is with the help of a home-made PSoC-based ATE. From the academic/research point of view, the ATE is a suitable tool to collect experimental data, to verify the fulfillment of design specifications, to enhance lumped design models, and to define novel test strategies as well. These are the reasons why the proposed ATE was mainly conceived for microelectronics education and research. In education, the ATE is the way to experience the complexity of real silicon ICs by integrating and testing topics described in graduate courses. For research, on the other hand, the ATE allows to verify the performance of circuits and devices according to design specifications given by several applications.

In this paper, the usefulness of the ATE has been demonstrated by showing experimental results of both commercial MOS transistors and integrated MOS transistors. The first one is a common device not only for laboratory activities, but also for identifying basic operations regions as well as for obtaining physical parameters via experimental data. The second one, on the other hand, is the basic cell to design silicon-based mixed-mode circuits and systems. However, even when either the commercial transistors' data sheet or SPICE simulations is the way to visualize the current-voltage characteristic and/or the transistor's basic parameters, running a setup designed for test needs and analyzing experimental data is an experience that allows us to evaluate the complexities of real devices. Unfortunately, such an experience is just a good wish when laboratory facilities are not enough to perform basic electrical characterization of devices. To face that difficulty, the Design Group has designed a portable, low-cost, PSoC-based ATE for academic and research activities. Fig. 7 shows several pictures where students test some circuits and/or devices with the help of the ATE. This figure shows several connections including power supply, PC, and LCD.

Figure 7. At the top, left hand, the ATE with external connectors is shown. Note that laboratory activities use a protoboard, which is a common tool used for constructing a circuit based on commercial components.

The ATE is a useful test board and it is still under development. In practice, new laboratory activities are demanding the development of other functions, where these functions do not need to increase existing external resources. Currently, the ATE offers programmable capabilities, memory, functions generator, current/voltage measurements (ac and dc), current/voltage sources (ac and dc), ports to download data from memory to a PC, frequency measurements, and external peripherals to build test master-slave architectures by using laboratory equipment. The ATE constitutes the Design Group's response to face the measurement process within all the design cycle: analysis, design, simulation, layout, post layout simulation, fabrication, and electrical characterization. Finally, it is important to mention the wide communication between the author and the PSoC's manufacturer not only for the comprehension of the PSoC performance, but also to correct data from the PSoC's data sheet. From such communication, a technical note describing both the architecture and usefulness of an ATE based on the PSoC is currently on line [14].

6. ACKNOWLEDGMENTS

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Author Biography

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Was born in San Luis Potosí, Mexico. He received the B.E. degree in Physics-Electronics from the USLP in 1988, Mexico, and the D. Sc. degree in electronics from INAOE, Mexico, in 1997. From 1991 to 1996, he worked in the at Microelectronics Laboratory at INAOE as a researcher developing wet-etching techniques and designing CMOS circuitry for silicon-based microsensors. In 1997, he was at CNM, in Bellaterra (Spain), as a visiting researcher being involved in the development of surface micromachining techniques to design a fully-integrated microphone. In 1999, he joined CINVESTAV, Guadalajara Unit, Mexico. From 2002 to 2006 he was the coordinator of the Electronic Design Group. His research areas include silicon-based sensors development, low-voltage low-power circuits design, silicon-based DC-DC converters and mixed-mode circuits for both RFID applications and multi-standard communications.