

Design, at transistor level, of a neuron with axonic delay

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ABSTRACT

An electronic neuron designed with only transistors, with the idea of being able to develop to future a VLSI integrated microcircuit is presented. The neuron is of leaky integrator type, with a ramp function with saturation type response and axonic delay. In this work we will present the mathematical model of our neuron, and its electronics main characteristics, as fundamental part of our simulation system, the neural analog computer.

RESUMEN

Se presenta una neurona electrónica diseñada con puros transistores con la idea de poder desarrollar a futuro un microcircuito integrado VLSI. La neurona es del tipo integradora, con respuesta tipo rampa con saturación y retardo axónico. En este trabajo presentamos el modelo matemático de nuestra neurona y sus características electrónicas principales, como parte fundamental de un sistema de simulación, la computadora neuronal analógica.

Keywords: Biological neuron models, artificial neuron models, electronic neuron models.

1. Introduction

The study of biological neurons, which are made of linear and non-linear elements, is limited by classical experimental approaches. A way to overcome these limitations is to study those neurons from a theoretical point-of-view, using mathematical models of the neurons, such as those following the classical Hodgkin-Huxley formalism [1], [2], [3]. That statement is a key point justifying the development of the research in computational neuroscience. But software that numerically solves the model equations is also somehow limited by the computation time, and in that case, analog computation appears as an alternative solution to the neural models. Following initiative studies [4], [5], we have developed in the 2000s, many analog electronic models for the implementation of artificial neurons [6], [7], [8], based on the Mc Cullock and Pitts [9] and leaky integrator formalism. Equations are computed by analog integrated circuits technology, and run in real time the electrical activity of the neuron, i.e. its membrane potential

with a good level of accuracy by leaky integrator models and the axonic delay. Le Masson [10], [11] and Carver Mead [12] have shown in previous publications the validity of this implementation mode for artificial neurons. Those circuits represent a powerful tool to test and validate results from computational neuroscience with neurophysiology experiments, and applications in neural networks, A. Van Schaik [13]. Starting from the isolated chip computing the neuron analog model, we then can build a complete analog simulation system, which supports the artificial neurons and allows using a dedicated instrumentation and software interface. In this work we will present the mathematical model of our neuron, and its electronics main characteristics, as fundamental part of our simulation system, the neural analog computer.

2. Mathematical model of a neuron

The mathematical neuronal model used is based on three neural basic operations, two lineal and one not lineal. The two lineal operations

correspond to the dendrite and somatic operations that corresponds to the neuron confluence function. The first of these operations is implanted by means of internal product of the external signals (dependent of time) with the vector of synaptic weight (independent of time). The second lineal operation is implanted by means of a leaky integrator one characterized by an integration constant. On the other hand, the non lineal operation corresponds to the activation function that is a ramp with saturation that is a lineal function to lines in this case. Additionally to the output of the neuron, it is considered a delay in the time that represents the axonal delay.

This way, the mathematical model of the lineal operations is established in the following way:

$$\tau \frac{du(t)}{dt} + u(t) = z(t) = \sum_{i=1}^n w_i x_i(t) \quad (1)$$

where $x(t) = [x_1(t), \dots, x_n(t)]^T$ is the time dependent input n-dimensional vector, $z(t)$ is the time dependent dendrite input, $w = [w_1, \dots, w_n]^T$ is the time independent synaptic weight vector, $u(t)$ is the time dependent neuronal activity, and τ is the time constant in the neuron integrator. The activation function mapping neuronal activity $u \in (-\infty, \infty)$ to a neuronal output, that is to say, $y = \Psi(u)$.

In this model we are considering that our non lineal activation function is delayed in time, that is to say, $y(t) = \Psi[u(t - \rho)]$ where the positive parameter represents the neuron axonal delay, and function Ψ represents a ramp function with saturation that is

$$\Psi(u) = \begin{cases} a & \text{si } u \leq \beta_i \\ (u - \beta_i) \left(\frac{A - a}{\beta_s - \beta_i} \right) + a & \text{si } \beta_i < u < \beta_s \\ A & \text{si } u \geq \beta_s \end{cases} \quad (2)$$

where $A, a (A > a)$ are, respectively, the limits of superior and inferior saturation, β_i, β_s ($\beta_i < \beta_s$) are, respectively, the inferior and superior thresholds, and the term $(A - a) / (\beta_s - \beta_i)$ corresponds to the slope of the ramp.

In this work, it is considered that the neuron is stimulated by an external single signal, that is to say, we have that $z_{ext}(t) = I(t)$. This way, the behavior of this type of neuron is described by the differential following equation:

$$\tau \frac{du(t)}{dt} + u(t) = I(t) + wy(t - \rho) \text{ for all } t \geq t_0. \quad (3)$$

For resolving this type of mathematical model electronically, we can use an analog computer circuit based on a symmetrical transconductance operational amplifier, because this circuit has responses with the ramp characteristics that we need. This circuit is very similar to the sodium-potassium neuron circuit described by Sarpeshar, Watts, and Mead. [14]

3. Transconductance operational amplifiers (OTA) design

The circuit of Figure 1 is called Symmetrical Transconductance Operational Amplifier (OTA); in it, we can see that transistors T9 and T10 generate a current mirror in such a way that current i_b is reflected in i_b' . In a similar way, transistors T3 and

T4 constitute another current mirror which reflects current i_1 , in the i_1' . In turn, transistors T5 and T6 that configure another current mirror reflected i_1' in i_1'' . In such a way that current $i_1'' = i_1$.

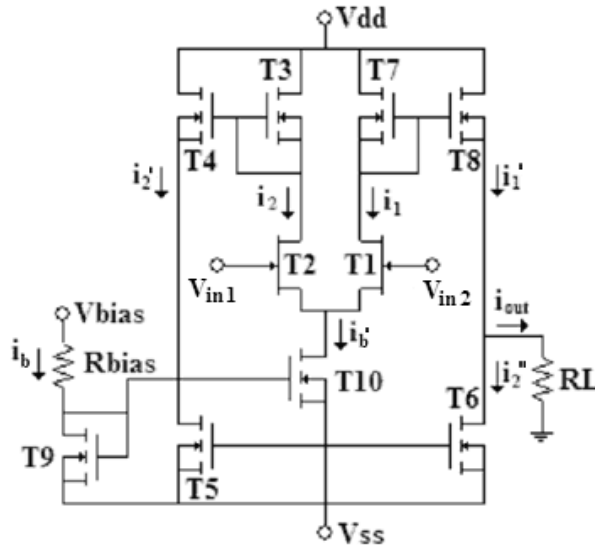


Figure 1. Symmetrical OTA

On the other hand, transistors T7 and T8 act as a current mirror that reflect the average i_2 in i_2' . Then we can say that the output current is similar to: $i_{out} = i_1 - i_2$, where i_1 and i_2 are the currents of FETs T1 and T2, in a way that the analysis carried out for the simplest OTA case is applicable to this symmetrical OTA, therefore, the output current will be

$$i_{out} = i_b \tanh \frac{k(v_{in1} - v_{in2})}{2} \text{ or } i_{out} = G_m(v_{in1} - v_{in2}) \quad (4)$$

In view of the fact that the output current is a hyperbolic tangent function of the input voltages difference, we can consider, within a certain values interval, output i_{out} like a lineal function. We implement the symmetrical OTA circuit shown in Fig. 12 with an average $i_{bias} = 6.412$ mA. The response of this circuit is shown in Figure 2.

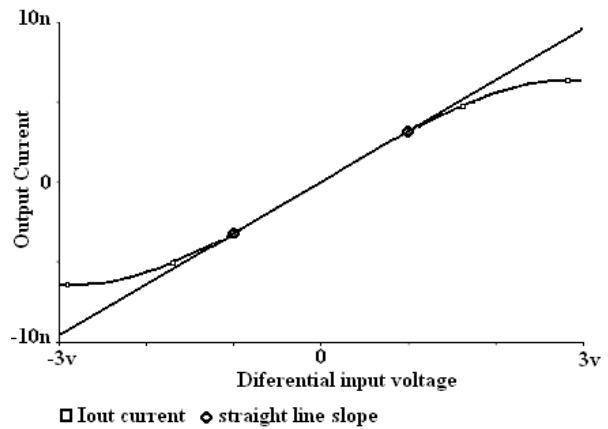


Figure 2. Symmetrical OTA output current

In Figure 2, we can see the OTA output current like a hyperbolic tangent, the one which compared with a straight line slope 0.0032 is almost lineal between the values of -1 and 1 Volts. If we remember that we want the ramp with saturation response, this type of amplifier is ideal for our model, in the same form that was considered by Rasche, C. [15].

3a. Comparison between proposed and commercial OTAs

It is convenient to compare the behavior of our OTA with some commercial circuit. To do this, we chose the operational transconductance amplifier LM13600 of National semiconductors [16] for the comparison. To compare the response of both circuits in the non inverter inputs, a ramp signal with amplitude that goes from -5 to 5 V, with a frequency of 1 KHz, will be applied while in the inverter inputs the amplitude will vary from 5 to -5 V, with the same frequency and phase. In both circuits we have a bias current of 4 mA, and the polarization voltages will be $V_{dd} = 10$ V and $V_{ss} = -10$. The load was a resistance of 100Ω. In Figure 3, we can appreciate that the linearity interval in the proposed OTA is bigger with respect to the commercial OTA.

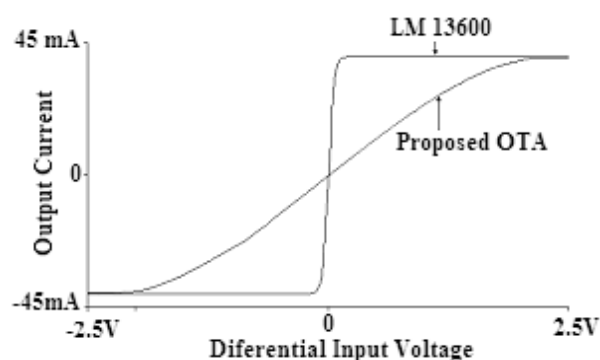


Figure 3. Comparison between the answer of the commercial OTA and the one proposed

4. Design of the confluence operation

The neuron mathematical model indicates that the confluence operation consists of three stages, first a weight stage, another aggregation stage and lastly one of threshold. In Figure 4, it can be seen as it is conformed the confluence operation in the analog circuit.

4a. Weight stage

In this stage the magnitude of each one of the input signals is pondered with a certain value in a way that we have the same input wave forms signals escalades in its magnitude at the output.

To implement this stage in an electronic way, we can make use of several operational transconductance amplifiers connected in a constant multipliers configuration. In Figure 5, we can see the schematic diagram of this stage.

4b. Aggregation stage

In our neuron mathematical model, this stage consists of two operations, one of sum followed by an integration one which produces the integration in time of the inputs sum, so much excitatory as inhibitory. We use the circuit shown in Figure 6 to implement this stage electronically.

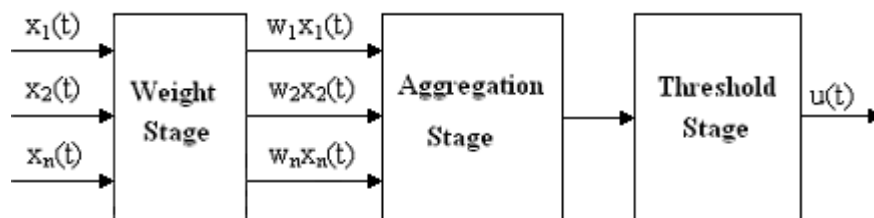


Figure 4. Confluence operation blocks diagram.

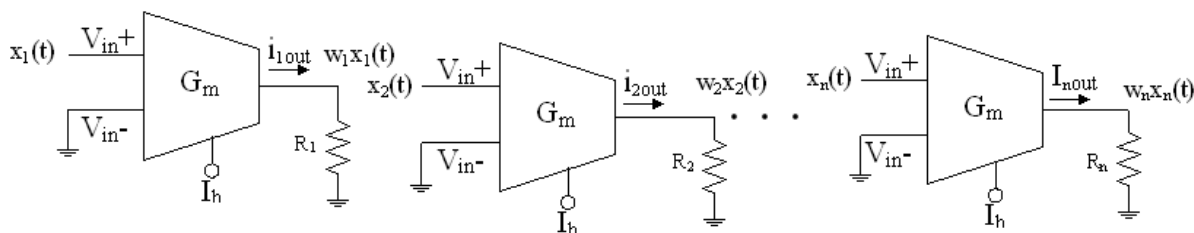


Figure 5. Weight stage schematic diagram

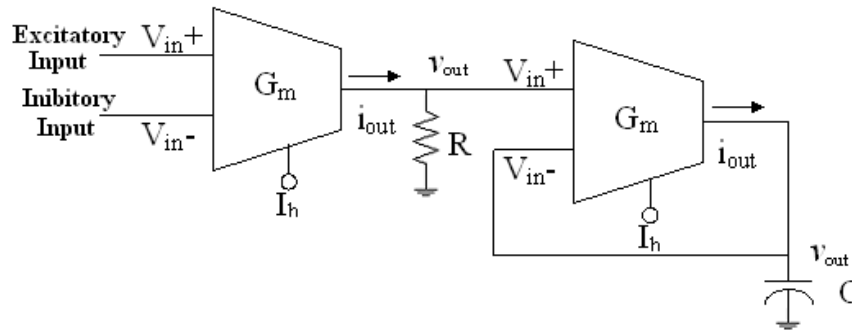


Figure 6. Aggregation stage

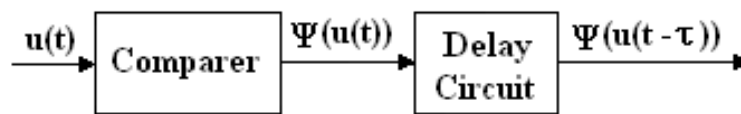


Figure 7. Activation operation blocks Diagram.

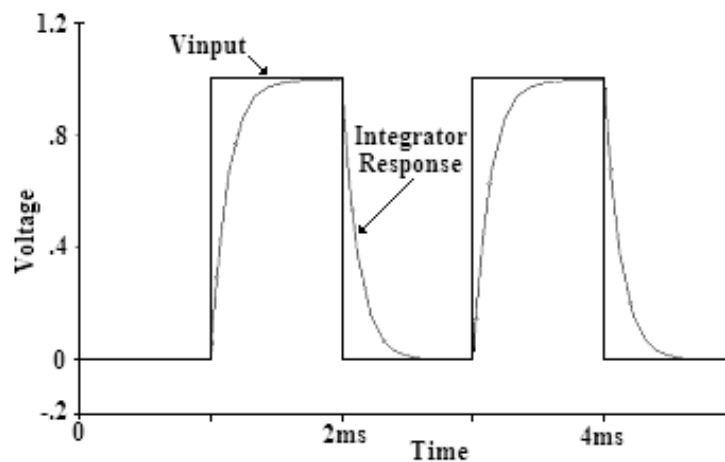
4c. Threshold stage

The threshold stage is the neuron stage in which we establish from what value the neuron will respond or will continue in rest. In particular, for the neuron that we are working with, this stage consists of a reference value provided by a voltage source that can be substituted by a voltage divider.

4d. Design of the activation operation

One characteristic of the activation operation is to be a non linear function. In our neuron case we opted for a step activation function. Additionally to this, the neuron response is delayed 1ms. The activation is formed as it is shown in Figure 7.

In Figure 8, the v_{out} behavior of the confluence operation is shown when the circuit is excited with a step signal.



Figures 8. Response of the integrator to a train of pulses.

5. Delay circuit

Our objective is to delay an asynchronous binary signal, and we propose to take advantage of the monostable circuits characteristic that generates a constant duration pulse when a change from low to high level is present. This way, if we have two groups of N monostables connected in series with the same constant of time, and we connect them to the input signal in such a way that the first monostable of a group shoots when the signal commutes from low to high, while in the other group this happens when the signal changes from high to low, what we will have in the monostable outputs will be two pulses at time t defaced equal to the input pulse width.

If we connect a slope edge detecting circuit to the output of each monostables group and, later, the

sequential circuit described in the previous section, we will be in possibility of building a duration pulse t starting from the pulses coming from the monostables. In this manner, the result will be a duration pulse t , defaced N times respect to the input pulse, which means that we have achieved our objective; this is to delay the initial pulse without modifying its characteristics. In Figure 9, the schematic diagram of this circuit is shown.

In Figure 10, the diagram of the complete delay circuit is shown.

In Figure 11, the complete neuron different stages that produce their behavior can be appreciated and correspond to the analog implementation of Equation 3.

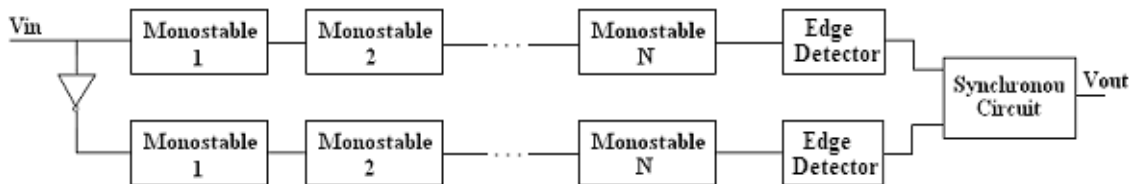


Figure 9. Delay circuit blocks diagram using N monostables.

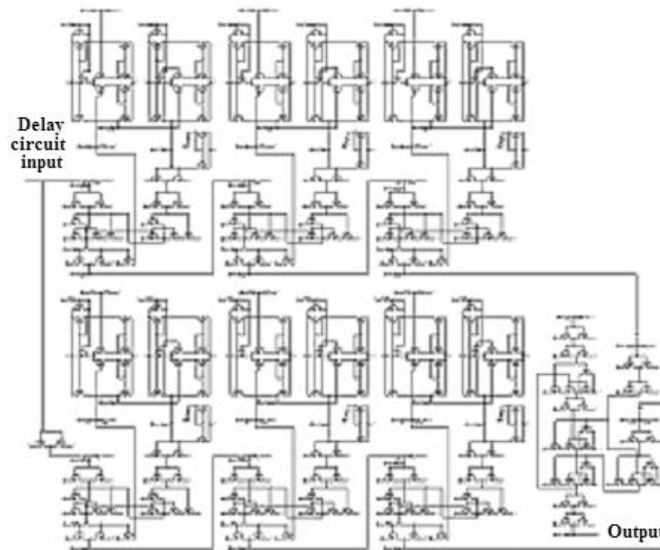


Figure 10. Proposed delay circuit

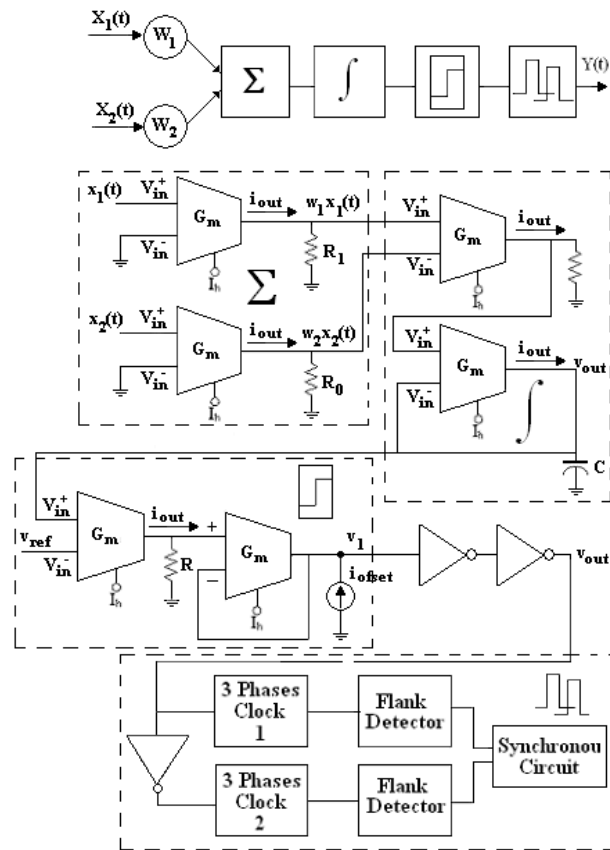


Figure 11. Complete analog implementation of Equation 3

6. Results

Once all the parts that form the neuron have been revised, we analyze the behaviour of the proposed

neuron. In Figure 12, an oscilogram, in which the two inputs appear as well as the response of some circuits that form it, is shown.

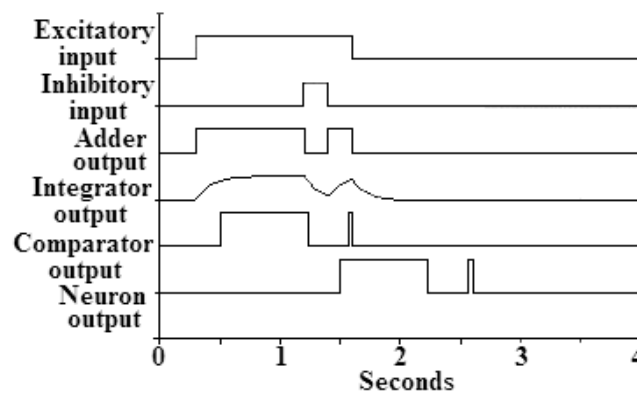


Figure 12. Response of the neuron and some of their parts.

In Figure 12, we can appreciate that in the adder output the subtraction of the excitatory signals excepting the inhibitory ones is obtained. This signal is integrated in the time and then, when being compared with a threshold level, it produces two square pulses of the same width but different duration. Later, these pulses are delayed a millisecond to produce the neuron response. The neuron is able to delay pulses of practically any duration without distorting them. The only circuit limit resides in the minimum separation between two up or down edges that must be distanced beyond $1/3$ of millisecond. In Figure 13, a graphic is shown; in such a graphic, the comparator output followed by the neuron response, which is a little different, appears; this results in the monostable simply ignoring the input, and this new pulse is not perceived by the neuronal response. This effect corresponds to the neuron refractory period.

Another situation that can happen is when, in the comparator output, two down edges are present in a smaller interval at $1/3$ of millisecond. This situation is illustrated in Figure 14.

We can see that two down edges are present in a smaller interval at $1/3$ of millisecond, the result is that the neuron response will remain in a high level until another pulse is presented and another down edge is detected.

In the 50s, Cragg and Temperley proposed, taking an analogy with the hysteretic phenomena observed in the ferromagnetic materials, that a located arrangement of neurons in certain cerebral regions could present a multistable behavior and give origin to a hysteretic response to periodic stimuli [17]. Different researchers have studied the mechanisms that can give origin to the hysteretic phenomena, both in big neural arrangements and in small circuits. In general, these studies have been based on considering the short term memory phenomenon as those neural processes that present a hysteretic response whose duration overcomes the stimulus that provoked it [18]. In Figure 15, the hysteric cycle generated as effect of the short term memory of the neuron for the signals of Figure 14 is shown.

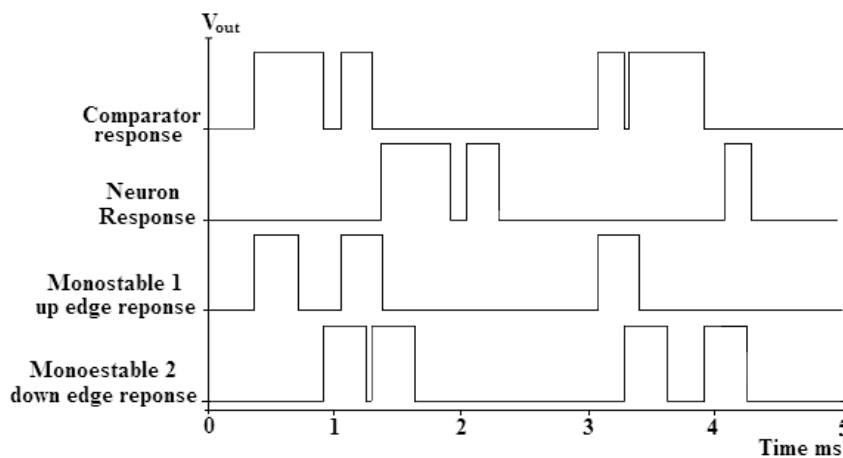


Figure 13. Neuron response when two up edges are present in the comparator output in a smaller interval at $1/3$ of millisecond

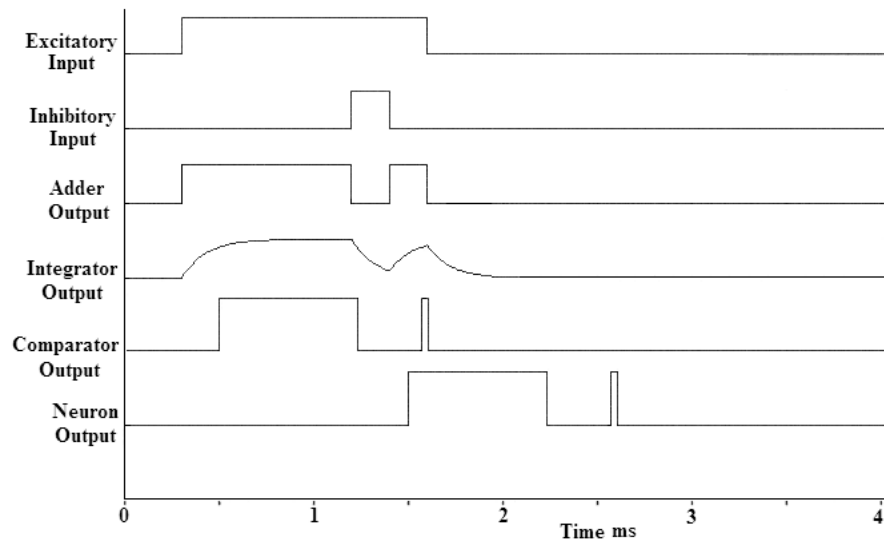


Figure 14. Neuron response when two down edges are present in the comparator output in a smaller interval at 1/3 of millisecond

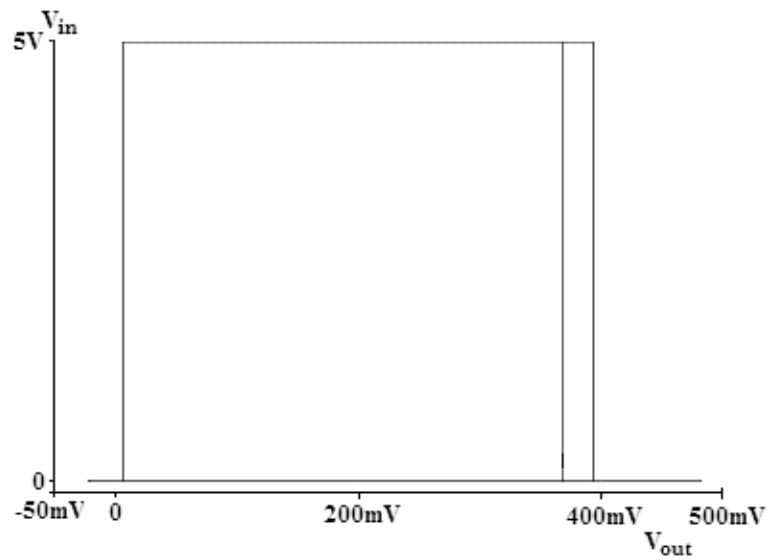


Figure 15. Short term memory effect

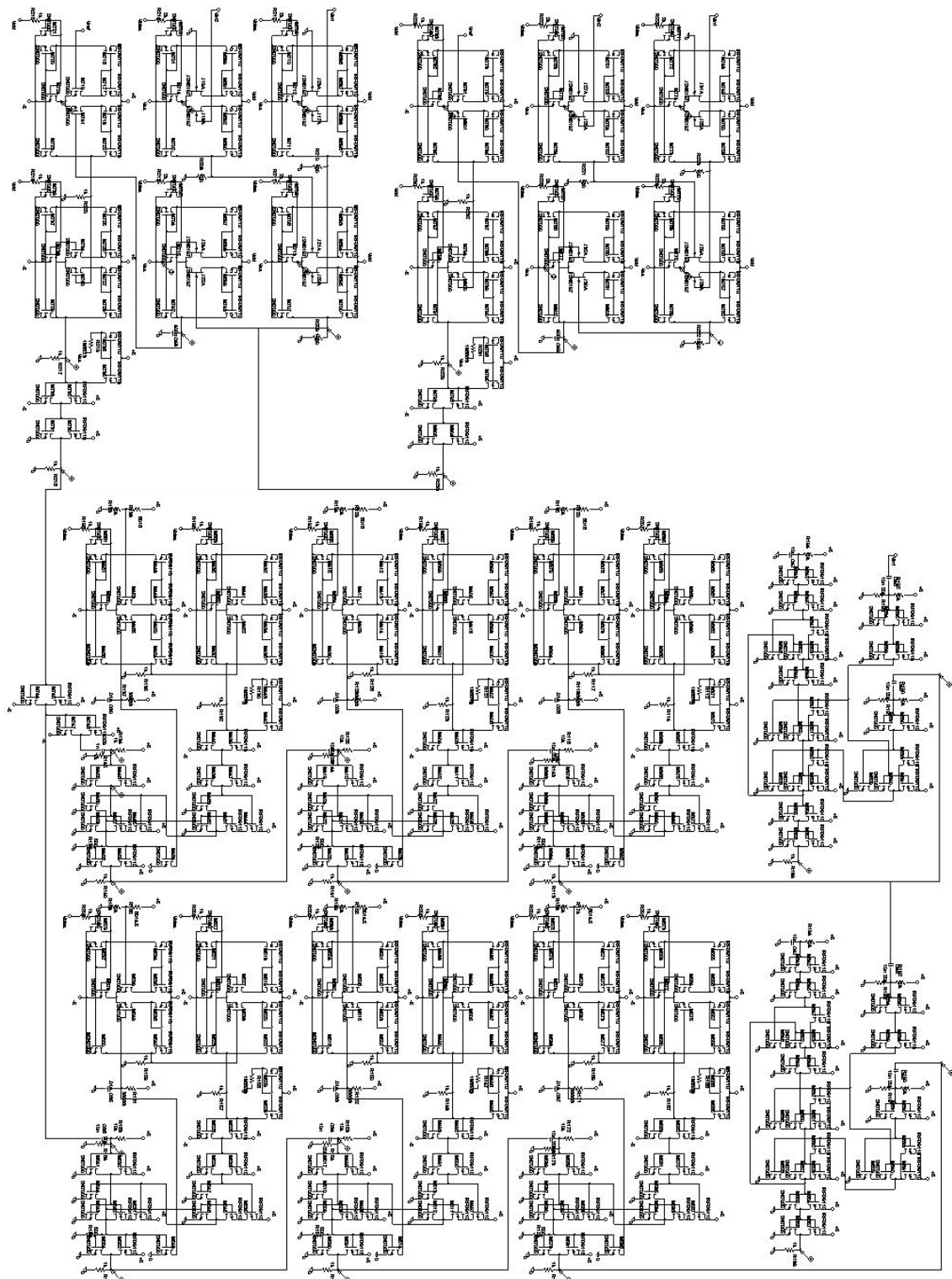


Figure 16. Complete neuron Schematic diagram

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