Design of an adaptive LNA for hand-held devices in a 1-V 90-nm standard RF CMOS technology: From circuit analysis to layout

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ABSTRACT

This paper deals the design of a reconfigurable Low-Noise Amplifier (LNA) for the next generation of wireless hand-held devices by using a lumped circuit approach based on physical laws. The purpose is not only to present simulation results showing the fulfillment of different standard specifications, but also to demonstrate that each design step has a physical meaning such that the mathematical design flow is simple as well as suitable for hand-work in both laboratory and classroom. The circuit under analysis, which is designed according to technological design rules of a 90nm CMOS technology, is a two-stage topology including inductive-source degeneration, MOS-varactor based tuning networks, and programmable bias currents. This proposal, with reduced number of inductors and minimum power dissipation, adapts its performance to different standard specifications; the LNA is designed to cope with the requirements of GSM (PCS1900), WCDMA, Bluetooth and WLAN (IEEE 802.11b-g). In order to evaluate the effect of technology parasitics on the LNA performance, simulation results demonstrate that the LNA features NF<1.77dB, S21>16dB, S11<-5.5dB, S22<-5.5 dB and IIP3>-3.3 dBm over the 1.85-2.48 GHz band. For all the standards under study the adaptive power consumption varies from 25.3 mW to 53.3mW at a power supply of 1-V. The layout of the reconfigurable LNA occupies an area of 1.8mm2.

RESUMEN

Este trabajo presenta el diseño de un amplificador de bajo ruido, LNA (del inglés *Low-Noise Amplifier*) reconfigurable para la siguiente generación de dispositivos portátiles de comunicación inalámbricos, usando la aproximación de circuitos concentrados sustentada en leyes físicas. El propósito de este trabajo no es sólo presentar resultados de simulación que muestran el cumplimiento de especificaciones para cada estándar, sino también demostrar que cada paso de diseño tiene un significado físico haciendo que el procedimiento matemático de diseño sea simple y adecuado para el trabajo a mano tanto para actividades en laboratorio como en el aula. El circuito bajo análisis, diseñado en una tecnología CMOS 90nm, consta de dos etapas que incluyen degeneración inductiva de fuente, redes de entonado basadas en varactores MOS, y corrientes de polarización programables. Esta propuesta, con reducido número de inductores y mínima disipación de potencia, adapta su desempeño a las diversas especificaciones de cada estándar; el LNA se diseña para cubrir los requerimientos de GSM (PCS1900), WCDMA, Bluetooth y WLAN (IEEE 802.11b-g). Para evaluar el efecto de las no idealidades de la tecnología en el desempeño del LNA, las simulaciones demuestran que el circuito cumple parámetros como NF<1.77dB, S_{21}>16dB, S_{11}<-5.5dB, S_{22}<-5.5 dB y IIP3>-3.3 dBm en la banda 1.85-2.48 GHz. Para todos los estándares bajo estudio, el consumo adaptivo de potencia varía de 25.3 mW a 53.3mW usando una fuente de alimentación de 1-V. El patrón geométrico del LNA reconfigurable consume un área de 1.8mm^2.

Palabras clave-Tecnología MOS, aplicaciones inalámbricas, circuitos reconfigurables

Index Terms-MOS Technology, wireless applications, reconfigurable circuits.

1. Introduction

The fourth generation (4G[1]) of wireless telecom systems will require a lot of high performance capabilities including low-power multi-standard chipsets, operation over a number of different communication protocols, signal conditions, battery status, etc [1]. These capabilities are the reason by which the efficient implementation of these systems demands for reconfigurable building blocks that can adapt to the different specifications not only with minimum power consumption, but also at low cost [2]. Up to now, the majority of multi-standard Radio-Frequency (RF) receivers use a single down-conversion scheme because both Intermediate-Frequency (IF) and Image Rejected (IR) filtering are eliminated in order to develop multi-standard architectures. The goal of such trend is a high hardware reuse specially by developing programmable and reconfigurable building-blocks [**3**]. Currently, one of the most challenging circuits is the LNA. The design of this circuit is especially critical due to its position at the receiver front-end, i.e. the LNA is closer to the antenna. Therefore, this circuit must not only match the antenna's impedance and amplify weak input signals with minimum noise contribution, but the LNA must also present high linearity and isolation from the rest of the receiver chain as well [**4**]. Furthermore, in the case of multi-standard applications, the proposed LNA must operate over different frequency ranges while keeping a reduced number of passives, i.e., capacitors and inductors, to increase the integration [1]-[**4**]. Then, to face the above-mentioned problems, the proposed LNA does not require switchable matching networks to select the resonant frequency nor additional passive components for the input and output matching networks [**5**]-[**15**]. The use of switches forces a discrete frequency selection, which is an expensive design option due to unwanted parasitic switch-on resistances; this effect increases the circuit noise. On the other hand, matching networks enhance the integration because inductors are omitted; unfortunately, these networks include resistors that increase also the circuit noise [**12**], [**15**]. So, in order to offer an alternative multi-standard LNA that solves the above-described noise problems, the proposed LNA adapts its performance to the requirements of four standards (GSM, WCDMA, Bluetooth and WLAN) with the help of two LC-networks to separately control the input impedance and the signal gain as well. In this proposal an MOS-varactor tuning array is used in both networks in order to make the resonance frequency programmable without penalizing the LNA noise

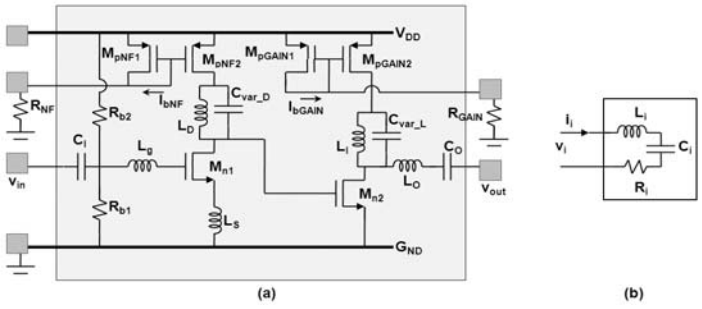

Figure 1.Tunable LNA proposal (a) and its ideal equivalent lumped circuit to match the input impedance (b).

[1] 4G systems will include services provided by 2G and 3G systems and additional applications where global positioning systems (GSP), metropolitan-, local-, and personal-areas networks are some examples.

performance. In order to evaluate the whole performance of the LNA, SpectreRF simulations considering technology parasitic have been widely carried out.

2. LNA Topology

Once the scenario has been described, Figure 1a shows the complete schematic of the proposed reconfigurable LNA. It consists of a two-stage topology with separate biasing circuits and tuning networks. Note that the input stage includes an LRC network needed to match the input impedance; the same is true for the output stage, where an LC network is included as well. The input stage uses an inductively degenerated common-source structure to provide a specified real part to the input impedance and signal gain at a given frequency whereas the output stage provides higher gain without significantly degrading the noise performance. Strictly speaking, this proposal adds several properties of well-known topologies in a unique reconfigurable architecture in order to minimize power consumption, reduce integration area and low cost by *paying* an extensive use of digital signal processing. Further, to enhance the advantages of this proposal, technological design rules of a modern nanoscale CMOS technology (1-V, 90nm) are used. CMOS technologies are expected to be the technological base of future hand-held devices.

In practice, since the interface between analog and digital circuitry is closer to the antenna, it is basic to analyze the LNA by satisfying an ohmic matching characteristic. Then, by assuming that a saturated MOS transistor, operating in a strong inversion, can be modeled by a Voltage-Controlled Current-Source (VCCS), and considering that inductors L_g and L_s are ideal, it is easy to show that the input impedance of the LNA in the Lapalce's domain is given by (1) where g_{mn1} and C_{gsn1} are the small-signal transconductance and gate-source capacitance of M_{n1}. The magnitude of Z_{in} (**s**) is obtained if **s** is replaced by jω, where [ω]=rad/s. Since at the resonant frequency the input impedance must be purely ohmic,

$$Z_{in}(s)=\frac{1}{sC_1}+\frac{s(L_g+L_s)+\frac{1}{sC_{gs}}+g_{mn1}\frac{L_s}{C_{gs}}}{1+\frac{1}{R_{b1}\|R_{b2}}\left[s(L_g+L_s)+\frac{1}{sC_{gs}}+g_{mn1}\frac{L_s}{C_{gs}}\right]} \quad (1)$$

$$Z_{in}(s)\approx\frac{L_g+L_s}{s}\left[s^2+\frac{1}{(L_s+L_g)(C_1+C_{gsn1})}\right]+\frac{g_{mn1}L_s}{C_{gsn1}} \quad (2)$$

$$Z_{eq}(s)=sL\|\frac{1}{sC}=\frac{sL}{s^2LC+1}=\frac{s}{C}\left(s^2+\frac{1}{LC}\right)^{-1} \quad (3)$$

$$\omega_r = \frac{1}{\sqrt{L_d C_{var\_D}}} = \frac{1}{\sqrt{L_l C_{var\_L}}} \quad (4)$$

Z_{in} is chosen to be equal to the RF source resistance, R_s. Furthermore, if the equivalent resistance $R_{eq}=R_{b1}||R_{b2}$ is chosen in such a way that the condition $R_{b1}||R_{b2}>>50\Omega$ is satisfied, (1) can be then simplified as shown in (2). This result shows that the real part of $Z_{in}(\mathbf{s})$ corresponds to $g_{mn1}L_s/C_{gsn1}$, i.e. $[Re(Z_{in})]=\Omega$. In this proposal, as the LNA is fully integrated as a stand-alone circuit, a termination of 50Ω is needed not only at the input terminal but also at the output one within the 1.85-2.48 GHz band. On the other hand, the tuning mechanism of the LNA is achieved by varying the resonance frequencies of the passive input/output tuning network.

The resonant frequency, ω_r, is easily calculated by analyzing the equivalent impedance of the parallel connection of an LC network, as shown in (3). From this result, it is easy to demonstrate that the input/output resonance frequency is given by (4), where $[L_{d,l}C_{var\_D,L}]=s^2$, and C_{var_D} and C_{var_L} are accumulation-MOS varactors provided by the 90-nm standard RF CMOS process used for the circuit implementation[2].

The capacitance of these varactors, controlled by voltages V_{Tl} and V_{TO}, could be varied from 20fF to 10pF in accumulation mode, providing a resonance frequency of up to 20 GHz. Note that, as each varactor is connected at the transistor drains of both stages, its noise contribution is attenuated by the gain of M_{n1} and M_{n2}. Further, since the gain of these transistors depends on the transconductance value, different bias current mirrors are used for biasing both stages in order to control separately the gain of M_{n1} and M_{n2}. In this way, the Noise Figure (NF) and the voltage gain of the LNA are individually controlled by using bias currents I_{bNF} and I_{bGAIN}, respectively. These currents are hence adapted to achieve the required specifications for each standard with the minimum power dissipation. In this proposal, bias currents are generated by external off-chip variable resistors, R_{NF} and R_{GAIN} (see Fig. 1), in order to prove the concept only. However, in a practical application, bias currents must be generated on-chip and controlled by the digital signal processor according to the required performance of the whole receiver. In addition to the bias currents, the gate of M_{n1} is biased by using a voltage divider made up of resistors R_{b1} and R_{b2}. These resistors, based on non-silicide polysilicon, are sized to provide the required operating point without degrading NF.

A. The Analysis Stage

The analysis of the proposed CMOS circuit shown in Fig. 1a corresponds to the *Analysis* stage of the design flow, where basic design models based on the lumped approximation have been used widely. The use of the lumped approach assumes that each electronic component represents just a physical characteristic, which does not depend on external/internal effects. Hence, the LNA analysis was carried out with the help of both Kirchhoff's laws and the Ohm's law. The later has been expressed in the Laplace domain by $V(s)=Z_e(s)I(s)$, where $Z_e(s)$ is the equivalent impedance for each electronic component, which corresponds to R, **s**L, and $(\mathbf{s}C)^{-1}$ for resistors, inductors, and capacitors,

[2] Note that **s** is the Laplace's variable, s denotes the basic unit of time and S corresponds to scattering parameters.

respectively. On the other hand, in conjunction with the lumped approach, the MOS transistor has been modeled as a simple VCCS in order to fulfill design specifications as well as multi-standard requirements. Note that the simplicity of the analysis does not represent a weak proposal, but a practical one supported in physical laws suitable for developing a transistor-level design procedure. However, for obtaining the electrical performance of design variables over the 1.85-2.48 GHz band, a simulation process is needed to evaluate the effect of parasitics on the LNA's performance and also to re-fine (if needed) the sizing of active/passive components. The characteristics obtained from simulation runs can not be deduced via hand-work due to the complexity of both the whole LRC-g_{mn} equivalent circuit and the resulting high order S-matrix. Note that the MOS transistor is modeled according to the lumped approach of that of the spice's LEVEL=1. This fact allows us to obtain performance results as close as those predicted by spice. That is the reason why electronic components could be re-sized to their optimal values.

B. The Synthesis Stage

Since the proposed reconfigurable LNA must satisfied several communication protocols, (2) is used to fulfill the requirements of the following standards: GSM (PCS1900), WCDMA, Bluetooth and WLAN (IEEE 802.11b-g). Table I summarizes these requirements that were extracted from a number of previously reported integrated receivers [**2**], [**4**], [**10**], [**16**], [**17**]. This table also shows specifications for the signal Band-Width (BW), LNA gain (S_{21}) and the third-order intermodulation intercept point, IIP3. So, to start the synthesis, it is possible firstly to study the ideal performance of (2) with the help of an equivalent circuit in order to analyze the ohmic matching characteristic for each standard. Such equivalent circuit is shown in Fig. 1b, where $L_i=L_g+L_s$, $C_i=C_I+C_{gsn1}$, and $R_i=g_{mn1}L_s/C_{gdsn1}$. Next, since the size of transistors is increased to minimize the NF, the aspect ratio of M_{n1} produces a parasitic C_{gs} of several tens of pF. Thus, if f_0 is defined as the frequency at which (2) is purely ohmic a design of experiments allows us to propose values for L_i and C_I in order to also minimize the integration area. As an example let us suppose a frecuenci 2.16GHz, L_i=12nH. With the help of (4) it is easy to verify that capacitor C_I is given by (5). This result produces, from the point-of-view of analysis, just the required ohmic impedance. In practice, since the expected input matching must satisfy S_{11}<-5dB for all the mentioned standards, C_I=7.13pF is actually the starting value to simulate the LNA in order to find not only the optimum value of the input capacitance, but also to satisfy matching requirements. However, the reader must not forget that the model $g_{mn1}L_s/C_{gsn1}$ must be taken into account in order to match the input impedance according to the condition S_{11}<-5dB.

Then L_s and L_g are at also variables under the designer control, i.e. $L_i=L_s(1+\alpha)$, where $\alpha=L_g/L_s$ is a fitting parameter.

$$C_I = \frac{1}{L_I\left(2\pi f_0\right)^2} - C_{gsn1} \approx 44.13\text{pF} - 37\text{pF} = 7.13\text{pF} \qquad (5)$$

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Standard	BW (GHz)	NF (dB)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)
GSM	1.85 – 1.99	1.7	11.5	<-5	-2
WCDMA	1.92 – 2.17	3.7	18	<-5	-0.5
Bluetooth	2.4 – 2.4835	28	12.5	<-5	-21
WLAN	2.4 – 2.4835	4.5	19.6	<-6	-5.4

Table 1 LNA specifications

C. The Design Stage

In order to cope with the different sets of specifications shown in Table I, the following design procedure has been followed:

- Passive elements of the input matching network (C_I, L_g, L_s) are derived from (2) in order to get the required input impedance, i.e. $|Z_{in}|=50\Omega$. Note that the input LRC network must cover a bandwidth defined by both the minimum frequency of GSM (1.85GHz) and the maximum frequency of WLAN and Bluetooth (2.4835GHz).

- Transistors M_{n1} and $M_{pNF1,2}$, and R_{NF} are sized in order to achieve the minimum value required for NF in the signal bandwidth, while trying to achieve the maximum voltage gain possible with the least power dissipation through proper adjustment of R_{NF}. At this design step, the values of R_{b1} and R_{b2} are set to provide the operating point required at the gate of M_{n1}, considering both linearity and noise requirements[3].

- Transistors M_{n2}, $M_{pGAIN1,2}$ and R_{GAIN} are sized in order to get the maximum voltage gain.

- The values of L_O and C_O are also calculated to get the output impedance matched to 50Ω.

- Components L_d, L_l, C_{var_D} and C_{var_L} are computed from (4) to get the required LNA tuning frequencies for each standard (see Table I).

- Technology parasitics are considered in an interactive electrical simulation process to re-fine the sizing and biasing obtained in the previous steps.

D. The Simulation stage

The outcome of the design procedure described above is the sizing and biasing of the LNA, summarized in Table II. The performance of the circuit has been adapted to the different standards specifications by varying the values of R_{NF} and R_{GAIN}. The final value of all components (including varactors) is shown in Table III. It is easy to corroborate that the voltage V_{GS} of both NMOS transistors is approximately 0.6V at V_{DD}=1V, while the optimal value of α is 122. On the other hand, note that L_S is approximately of the order of the bonding inductance. Thus, just four inductors are designed.

[3] By neglecting the effect of bias resistors and technology parasitics of passive elements, the NF of the LNA is approximately the same as that of the well-known inductively-degenerated common-source LNA [**4**].

Transistors	W/L (μm/μm)	Capacitors	(pF)	Inductors	(nH)	Resistors	(kΩ)
M_{n1}	180/0.1	C_I	7.7	L_d	1.6	R_{b1}	6
M_{n2}	180/0.2	C_O	7.7	L_g	12.2	R_{b2}	4
M_{pNF1}	1/0.1	C_{var_D}	2.7-4.3	L_s	0.1		
M_{pNF2}	300/0.1	C_{var_L}	0.7- 1.1	L_I	6.4		
M_{pGAIN1}	1/0.1			L_O	16.9		
M_{pGAIN2}	300/0.1						

Table 2 LNA sizing

Standard	R_{NF} (kΩ)	R_{GAIN} (kΩ)	I_{bNF} (mA)	I_{bGAIN} (mA)	C_{var-D} (pF)	C_{var-L} (pF)
GSM	0.5	2.5	32.4	20.4	4.3	1.1
WCDMA	3.4	0.5	25.8	2.4	3.9	1.0
Bluetooth	4.1	0.5	24.7	0.9	2.7	0.7
WLAN	3.1	0.5	26.6	3.6	2.7	0.7

Table 3 Parameter configuration for the different standards

3. Discussion of results

The LNA has been powered with a single 1-V supply voltage. In order to consider parasitics of passive components, the performance of the LNA has been extensively verified with the help of CADENCE SpectreRF. Fig. 2a shows the layout of the test chip, where the die area is 1.8mm^2 (including bonding pads), with the core occupying 1.0mm^2. A goal of this proposal, contrary to most reported multi-standard LNAs, is the reduced number of inductors. Fig. 2b represents the NF-frequency characteristic for all the standards under study. The overall minimum value of NF is 1.6dB, obtained at 1.85 GHz that corresponds to the lowest limit of the GSM band. Figs. 2c and 2d show, on the other hand, the forward-gain (S_{21}) and the input reflection coefficient (S_{11}), respectively. The minimum value of S_{21} is above 16dB, corresponding to Bluetooth, whereas S_{11} and S_{22} are below -5dB for all standards. On the other hand, the linearity of the LNA has been also taken into account in the design procedure. As shown in Fig. 3a (at the top), the minimum and maximum values achieved are -3.3dBm and 0.7dBm for WLAN and GSM, respectively. Finally, Table IV sums up the simulated performance of the LNA by showing the worst-case values of the different figures for each standard. This performance is compared in Table V with previous reported multi-standard CMOS LNAs, by using the following Figures Of Merit (FOM) [**18**]:

$$\mathrm{FOM}_1 = \frac{\mathrm{Gain}}{(\mathrm{NF}-1)\mathrm{Power}} \qquad (6)$$

$$FOM_2 = \frac{Gain \cdot IIP3 \cdot f_c}{(NF-1)Power} \quad (7)$$

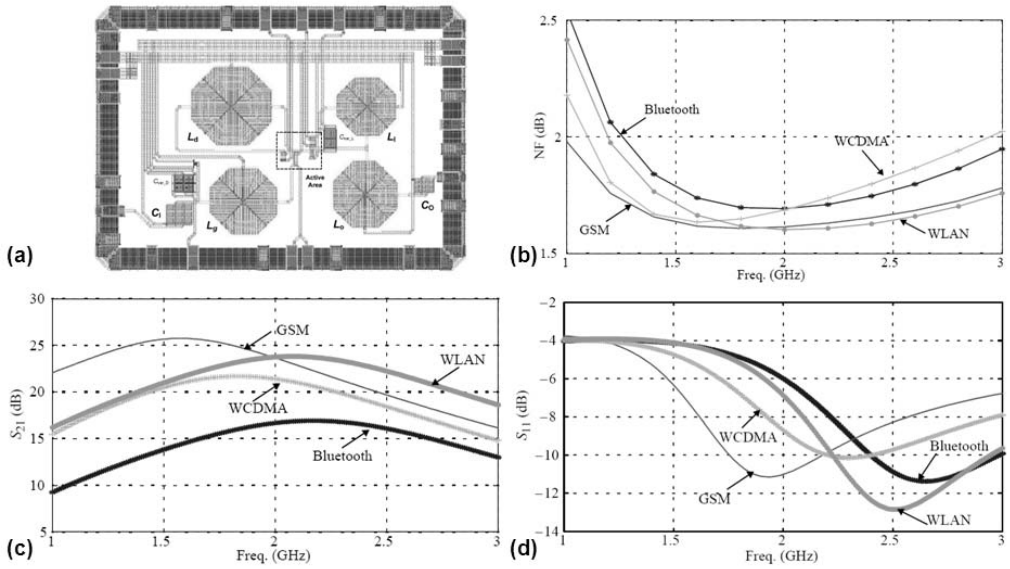

Figure 1. Layout of the LNA (a), and the performance of NF (b), S_{21} (c) and S11 (d) in the frequency

where f_c is the operating frequency of the LNA; [Power]=mW, [IIP3]=mW, [f_c]=GHz, while Gain and NF are dimensionless parameters. Note that the proposed circuit compares favorably to previous LNAs while covering a large number of standards. However, although the power consumption (especially in the GSM case) is higher than some

Standard (Band, GHz)	NF (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	IIP3 (dBm)	Power (mW)
GSM (1.85-1.99)	< 1.61	> 24.7	< -10.9	< -16.7	0.7	53.3
WCDMA (1.92-2.17)	< 1.73	> 20.6	< -7.9	< -5.5	-0.15	28.5
Bluetooth (2.4, 2.4835)	< 1.77	> 16.2	< -10	< -5.2	-0.6	25.3
WLAN (2.4, 2.4835)	< 1.64	> 22.3	< -12.4	< -6.3	-3.3	30.5

Table 4 Simulated performance summary of the LNA

other designs, it should be noticed that this is a direct consequence of the reduced value of the NF reported. Indeed, depending on the receiver specifications, signal conditions and/or battery status of the receiver, the proposed LNA can adapt its power consumption by reconfiguring its bias currents. This is illustrated in Fig. 3a (at bottom), where the NF-I_{bNF} characteristic is presented. Note that NF can be varied from around 1.55 to 4 by reducing I_{bNF} from ~27mA to 17mA at the price of reducing S_{21} by ~6 dB. On the other hand, NF can be kept constant (around ~1.6 dB) by increasing I_{bNF} if a higher gain value is needed.

4. Conclusions

The lumped-approach based design and electrical implementation of a multi-standard LNA in a 90-nm RF CMOS technology has been presented. Simulation results (CADENCE Spectre RF) demonstrate that the use of reconfigurable bias currents and MOS-varactor based tuning networks effectively allows the LNA to adapt its currents and MOS-varactor based tuning networks effectively allows the LNA to adapt its performance to the specifications of GSM, WCDMA, Bluetooth and WLAN standards. Transistors-level simulations including technology parasitics verify an acceptable performance showing a good comparison with previous reported designs. It is important to mention that, although some LNAs in Table V (including this proposal) do not report experimental results, they are included in the comparison study for the sake of completeness. Those references marked with an * in Table V correspond to integrated circuits showing experimental measured performance. Currently the test chip is under fabrication. Future work includes not only the design of a suitable PCB-based setup for testing the performance of the LNA for each standard, but also experimentally demonstrate that the use of both reconfigurable loading and PMOS – varactor based tuning is a new methodology because of the reduced number of inductors.

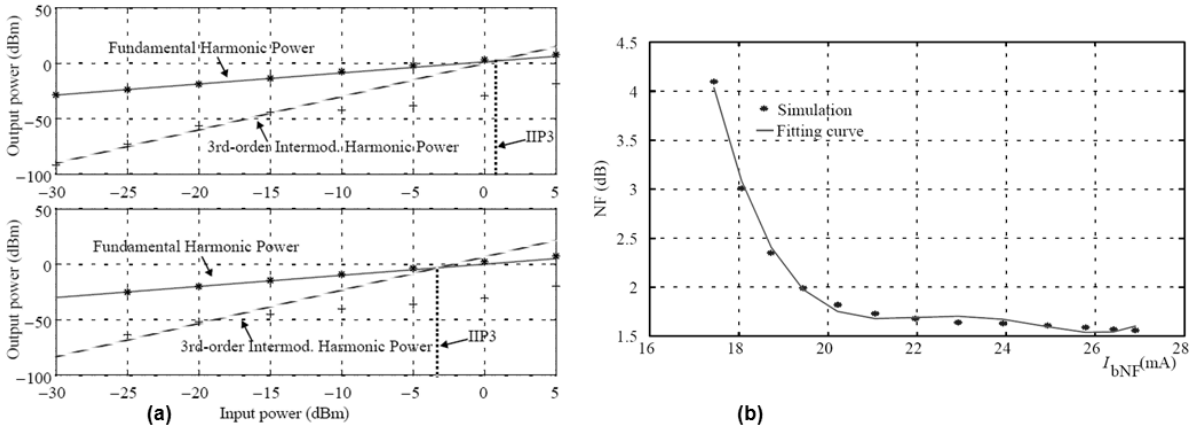

Figure 3. IIP3 for GSM and WLAN (a) and NF vs I_{bNF} (b) domain.

Reference	Standard	NF (dB)	S_{21} (dB)	IIP3 (dBm)	f_c (GHz)	Power (mW)	FOM_1	FOM_2
[6]	Bluetooth	2.2	15	3.0	2.4	7.2	1.2	5.7
	DECT	2.3	17	0.5	1.9	14.4	14.4	1.5
[8]	WLAN 802.11b-g	2.3	14	-1.5	2.4	50	0.1	0.01
	WLAN 802.11a	4.4	13	-1.5	5.3	50	0.05	0.2
	WiMAX	3.2	13.9	-10	3.5	50	0.09	0.2
[9]	WCDMA	3.9	23.3	-6.3	2.1	9.0	1.1	0.5
	GSM	2.6	24.9	-21.6	0.95	9.0	2.4	0.02
[10]*	DCS1800	5.2	28.5	-7.5	2.1	24	0.5	1.0
	WCDMA	5.6	23.4	0	2.4	24	0.2	0.2
	WLAN	5.8	23.4	-4.8	1.8	24	0.5	0.2
This work	WCDMA	1.73	20.6	-0.15	2.04	28.5	0.8	1.5
	Bluetooth	1.77	16.2	-0.6	2.44	25.3	1.5	1.1
	WLAN	1.64	22.3	-3.3	2.44	30.5	0.9	1.1
[15]*	0.3-2 GHz	4.5	12	-16	1.15	18	0.1	0.003

Table 5 Comparison with several reported multi-standard CMOS LNAs

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