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Use of boost power stage for static voltage gain improvement of a non-isolated continuous input current three-level DC-DC converter

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Abstract: The work presented in this paper describes the steady state analysis of a non-isolated and continuous conduction mode (CCM) operated three-level DC-DC converter with input boost power stage for achieving high static voltage gain. The proposed converter configuration is a double boost DC-DC conversion scheme. A boost power module consisting of a power switch, an inductor, a pre-charge diode, and a diode rectifier is introduced as the input stage in the conventional three-level DC-DC converter configuration to obtain the DC-DC converter topology suggested in this research work. The role of the input boost power stage is to extend the voltage gain of the conventional three-level boost converter. The proposed topology employs two power switches in addition to a boost power switch with simple control strategy so that the switching losses are reduced. The switches are subjected to low voltage and current stresses. The suggested non-isolated converter is operated under continuous inductor current mode in open loop configuration. The converter configuration has been simulated in MATLAB / SIMULINK platform. The input boost power stage receives a voltage of 24 V from a DC source. With low duty ratio (= 0.8) of the power switches, a DC voltage of around 208 V is obtained at the load end. The passive components of the converter are so designed that the filtering requirements on the DC output voltage and current waveforms are reduced. The voltage gain of the proposed converter is compared with that of the three-level boost converter without input boost power stage. The various modes of operation of the suggested converter are discussed with relevant equivalent circuits. The proposed system is validated using a developed hardware prototype model of 100 W converter with a low cost KA3525A PWM controller. Both simulation and prototype model results demonstrate that the proposed converter suits for high voltage gain applications.

Keywords: Boost power stage, CCM, Duty ratio, MATLAB/SIMULINK, Prototype model, PWM controller, Three-level Non-isolated DC-DC converter, Voltage gain

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1. Introduction

To generate bulk amount of AC electrical energy, fossil fuels have been used for centuries. But, the use of fossil fuels such as coal, natural gas, and petroleum, leads to serious environmental contaminations, public health issues, and increased cost of the power generation systems. Moreover, the existing fossil fuels are fast depleting and non-renewable. Due to the above drawbacks of conventional non-renewable energy systems, the researchers concentrated on an alternate scheme called the renewable form of power generation systems. One of the renewable energy sources like photovoltaic (PV) modules can be used to generate electrical energy in the form of DC. However, the DC output voltage from the PV source is low, and fluctuating due to the changes in sun irradiation and temperature. The low level DC output voltage of the PV source can be converted into a high level DC output voltage using an intermediate high gain DC-DC power electronic converter. This high level DC output voltage is to be fed to a grid connected inverter for producing AC electrical power. Hence, an appropriate high voltage gain DC-DC conversion stage needs to be developed with significant features of reduced voltage-current stress for the power switches and low ripples in the input current.

High voltage gain DC-DC converters can be divided into isolated and non-isolated topologies (Behera et al., 2020; Chen et al., 2019; Dobi & Sahid, 2020; Forouzesh et al., 2018; Girija & Murali, 2021; He & Khaligh, 2017; Mumtaz et al., 2021; Murali, 2021; Murali & Annapurani, 2019; Murali & Annapurani, 2021; Saravanan & Ramesh Babu, 2019; Shahir et al., 2017; Shahir et al., 2019; Siddharthan & Balasubramanian, 2019; Sowmya & Murali, 2019; Wang et al., 2019). The DC input and DC output ports are isolated using a high frequency transformer in the case of isolated DC-DC converter configurations where high voltage gain proportional to the kVA rating of the transformer can be achieved. But the overall efficiency of the transformer-based converter topologies is reduced due to certain factors such as (i). voltage spikes on the power switches due to the transformer's leakage inductance and higher amount of power dissipation, (ii). electromagnetic interference (EMI) problems. The structure and the control of the isolated configurations are also complicated. However, the simplified structure, high efficiency and the simple control of the non-isolated DC-DC converter configurations make it more desirable for electric vehicle (EV) applications (Chen et al., 2019; Wang et al., 2019).

The conventional two-level single-switch DC-DC boost converter can achieve high voltage conversion ratio at duty cycle value nearer to unity (Hsieh et al., 2013; Hua et al., 1994). But the high duty ratio results in reduced efficiency of the converter due to the increased conduction and switching losses. Another way of obtaining high voltage gain is by connecting a number of boost converters in series, which may lead to the high cost of conversion scheme.

A large voltage gain applied to fuel cell can be achieved using quadratic boost converter topologies (Leyva-Ramos et al., 2017; Wang, Qiu et al., 2019). But, these topologies have a relatively large amount of switching power losses due to high voltage stress occurring in the transistors. Some authors proposed a coupled inductor based quadratic boost DC-DC converter with high voltage gain and reduced switch voltage stresses (Lee & Do, 2019). The high voltage gain can also be achieved using multilevel converter topologies in which the transistors have lower voltage stress. However, the multilevel topologies have the disadvantage that more number of semiconductor devices needs to be used (Jiang et al., 2018).

Non-isolated non-coupled inductor based DC-DC converter topologies have also been used to achieve high voltage gain (Annapurani & Murali, 2020; Arab & Shokrollahi, 2019; Varesi et al., 2017). Due to the absence of magnetic components, the non-coupled inductor based DC-DC converter structures can produce high voltage gain with high power density and better efficiency. To improve the voltage gain of the converter, the switched-inductor (SI) and switched-capacitor (SC) based DC-DC converters with transformerless structures are also used, where the major issues are the high current and voltage stresses occurring on the power switches (Ajami et al., 2015; Jiao et al., 2011; Kim et al., 2019; Stala et al., 2019; Wu et al., 2015). Hence, the coupled inductor approach was used to achieve high voltage conversion ratio (Axelrod et al., 2015; Liu et al., 2016; Mulla et al., 2021). However, the coupled inductor structures have the disadvantage that the power switches are subjected to high voltage spikes due to the leakage inductance of the inductor. The switching losses are also increased. But, this issue can be resolved using an active clamp circuit (Liu & Li, 2016).

To resolve the issues present in the converter topologies discussed in the above literature survey, a non-isolated three-level DC-DC boost converter topology has been suggested for obtaining a high voltage gain (Balakishan et al., 2015). The converter structure proposed in (Balakishan et al., 2015) has the same voltage gain as that of the conventional two-level boost topology. But, in three-level structure, the inductor has the reduced size and the voltage rating of the power switch is reduced to half of the output DC voltage. Hence, the switches are subjected to low voltage stress thereby reducing the switching losses. Hence, this paper proposes a non-isolated three-level DC-DC converter topology with input boost power stage so that the voltage gain is improved by (1+D) times that of the conventional two-level topology, where D is the duty ratio of the power switch. The converter proposed in this work is a double boost topology. The voltage gain of the proposed converter operating in continuous conduction mode is same as that of the non-isolated double boost DC-DC converter

suggested in (Liu et al., 2020). In (Liu et al., 2020), the converter has the drawback that the voltage stress across the switch in the second boost stage is same as that of the conventional two-level boost converter. Whereas, in this research work, each switch at the output side is subjected to the voltage stress of half of the output voltage only. A prototype model of the converter configured as double boost topology has also been developed to validate the simulation results. The switches are subjected to low current stress.

The organization of the remaining sections is planned as follows: The topology and the modes of operation of the proposed converter are discussed in Section 2. Section 3 presents the MATLAB simulation results for the purpose of validating the proposed non-isolated positive output DC-DC converter. The developed prototype hardware model and its results for the proposed topology are discussed in Section 4. This is followed by the conclusions in Section 5.

2. Configuration and modes of operation of the proposed positive output three-level DC-DC converter

The configuration of a non-isolated positive output DC-DC boost converter with high voltage gain capability is shown in Figure 1. The suggested topology is the extension of the converter configuration given in (Balakishan et al., 2015) with boost power stage included. The converter is operated in continuous conduction mode. The proposed configuration employs passive components such as two identical inductors (L_b and L) each of 1 mH inductance, and two identical capacitors C_1 and C_2 each of 200 µF capacitance. The capacitors C_1 and C_2 are selected so that the balancing of voltage is achieved across the capacitors. The suggested topology is a double boost configuration. The first stage is a boost power stage consisting of boost switch (S_b), boost inductor (L_b), boost pre-charge diode (D_b), and a boost rectifier diode (D_{br}) with DC source (V_{in}). The second stage is another boost power stage comprising of power switches (S_1 and S_2), two ideal diodes (D_1 and D_2), and the capacitors C_1 and C_2 respectively. Each of the capacitors C_1 and C_2 receives half of the output voltage (V_0) and are acting as filter capacitors to filter out the ripples in the DC output voltage and current. The ideal power switches (S_b, S_1, and S_2) are suitably triggered into conduction by proper gate pulses with duty ratio D = 0.8 for each switch. The switching frequency (f_s) of the switches is taken as 50 kHz. The four distinct modes of operation of the converter are discussed as shown in Figure 2. The key waveforms of the converter configuration proposed are shown in Figure 3.

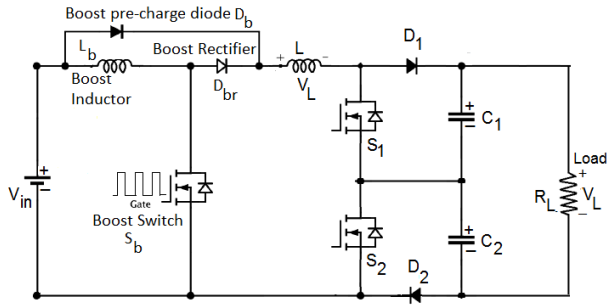
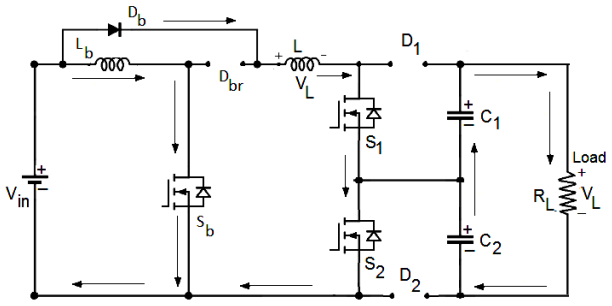
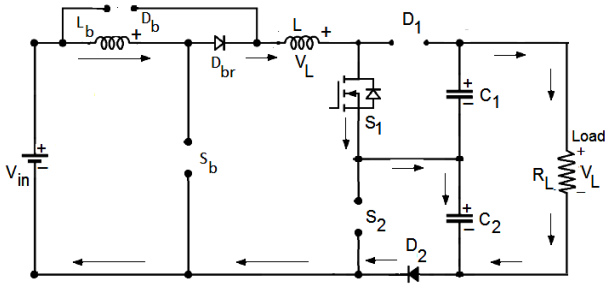


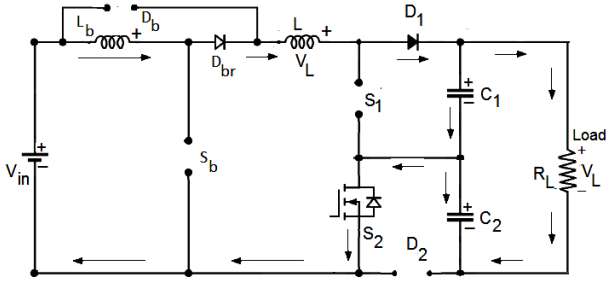
Figure 1. Circuit configuration of the proposed non-isolated three-level DC-DC boost converter.



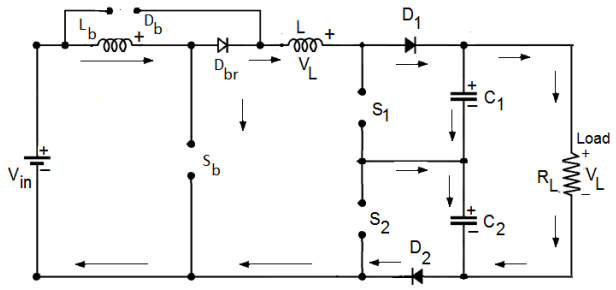
(a). Mode-I ($t_0 < t < t_1$)



(b). Mode-II ($t_1 < t < t_2$)



(c). Mode-III ($t_2 < t < t_3$)



(d). Mode-IV ($t_3 < t < t_4$)

Figure 2. Modes of operation of the converter: (a). Mode I, (b). Mode II, (c). Mode III, (d). Mode IV.

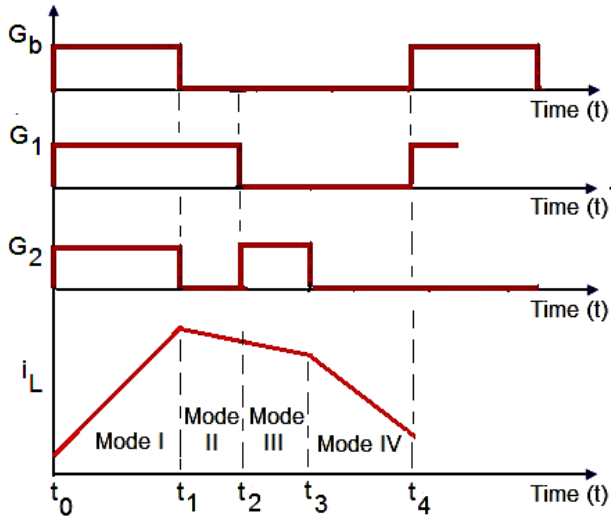


Figure 3. Key waveforms of the suggested converter for 0.5 < D < 1 during continuous inductor current mode.

2.1. Mode-I ($t_0 < t < t_1$)

The Mode I operation of the converter is depicted in Figure 2(a). In this mode, the switches S_b, S_1, and S_2 are turned ON. The diode D_b gets forward biased. The diodes D_{br}, D_1, and D_2 are reverse biased. The two inductors L_b and L are charged to the supply voltage V_{in} (>0) since they are connected in parallel. The two identical inductors L_b and L carry equal currents and they absorb the energy (W_{ON}) from the DC source. The charged capacitors C_1 and C_2 supply the load current. The current flow path is as indicated in Figure 2(a). The following equations are obtained during Mode-I operation:

$$V_{L_b} = V_L = V_{in}\ ;\ I_{L_b} = I_L\ ;\ V_{C_1} = V_{C_2} = \frac{V_0}{2} \tag{1}$$

$$W_{ON} = V_{in} I_L D T_s \tag{2}$$

Where, V_{L_b}, V_L and V_{in} represent the voltages across the inductors L_b and L, and the input DC voltage respectively; $I_{L_b} = I_L$ = current through the inductor L_b = current through the inductor L; V_{C_1}, V_{C_2} = voltage across capacitor C_1 = voltage across capacitor C_2; V_0 = output DC voltage; W_{ON} represents the energy absorbed by each inductor during turn ON period of all the switches; D is the duty cycle of Pulse Width Modulation (PWM) pulse for each switch (Assume that all the three S_b, S_1, and S_2 have the same duty ratio D; and T_s is the PWM period of the pulse.

2.2. Mode-II ($t_1 < t < t_2$)

During this time interval, the switch S_1 remains in the turn ON mode. The switches S_b and S_2 are turned OFF. The diodes D_b and D_1 are reverse biased. The diodes D_{br} and D_2 get forward biased. The current flow path is as indicated in Figure 2(b). The two inductors are connected in series. The voltage appearing across each inductor is given by Eq. 3.

$$V_{L_b} = V_L = \left(\frac{V_{C_2} - V_{in}}{2}\right) \tag{3}$$

This voltage level is so low that only small amount of energy is released from the inductors L_b and L through S_1 and C_2 for 0.5 < D < 1 as shown in Figure 3.

2.3. Mode-III ($t_2 < t < t_3$)

During this time interval, the switch S_2 is turned ON. The switches S_b and S_1 are turned OFF. The diodes D_b and D_2 are reverse biased. The diodes D_{br} and D_1 get forward biased. The current flow path is as indicated in Figure 2(c). The two inductors are connected in series. The voltage appearing across each inductor is given by Eq. 4.

$$V_{L_b} = V_L = \left(\frac{V_{C_1} - V_{in}}{2}\right) \tag{4}$$

This voltage level is also so low that only small amount of energy is released from the inductors L_b and L through C_1 and S_2 for 0.5 < D < 1 as shown in Figure 3. The voltage levels across the two inductors are equal during Mode II and III since $V_{C_1} = V_{C_2} = \frac{V_0}{2}$.

2.4. Mode-IV ($t_3 < t < t_4$)

During this mode, all the switches (S_b, S_1, and S_2) are turned OFF. The diode D_b gets reverse biased. The remaining diodes are forward biased. The current flow path is as indicated in Figure 2(d). The two inductors are connected in series. The voltage appearing across each inductor is given by Eq. 5.

$$V_{L_b} = V_L = \left(\frac{V_0 - V_{in}}{2}\right) \tag{5}$$

This voltage level is sufficiently high that major amount of energy is discharged from the inductors L_b and L through (i). the series combination of C_1 and C_2, and (ii). the load R_0 as shown

in Figure 3. The energy released (W_{OFF}) by each inductor is given by Eq. 6.

$$W_{OFF} = \left(\frac{V_0 - V_{in}}{2}\right) I_L (1 - D) T_s \quad (6)$$

According to the law of conservation of energy, the Eqs. 2 and 6 are equal. Hence, the voltage gain (G) of the proposed DC-DC converter is obtained as shown by Eq. 7.

$$G = \frac{V_0}{V_{in}} = \frac{1+D}{1-D} \quad (7)$$

3. Simulation results and discussion

The MATLAB / SIMULINK model of the proposed non-isolated continuous inductor current mode operated three-level DC-DC converter with boost power stage is developed and is shown in Figure 4. The boost power stage consists of a power switch S_b, an inductor L_b, a diode D_b, and a boost rectifier diode D_{br}. The switching frequency (f_s) for the converter is chosen as 50 kHz with duty ratio D = 0.8 for each switch. The values of converter parameters used for simulation are shown in Table 1. Each of the three switches (S_b, S_1, S_2) is triggered into conduction by applying the gate pulse as shown in Figure 5. The converter circuit is energized by a DC input voltage (V_{in}) of 24 V as shown in Figure 6. The current (I_{in}) delivered by the input DC source is as shown in Figure 7. With duty ratio D = 0.8 for each switch, the voltage obtained at the load end (V_0) is around 208 V and the load current (I_0) is nearly 0.66 A as depicted in Figure 8 and Figure 9 respectively. But, without the boost power stage, the output voltage (V_0) is around 120 V and the corresponding output current (I_0) is nearly 0.38 A for the same input DC voltage and duty ratio (Balakishan et al., 2015). Hence, the voltage conversion ratio as well as the output current of the converter proposed in this research work have been enhanced. The boost inductor (L_b) voltage and current waveforms are shown in Figure 10 and Figure 11 respectively. Similarly, the waveforms of voltage across and current through the inductor L are depicted in Figure 12 and Figure 13 respectively. The voltage stress and current stress of the power switches S_b, S_1, and S_2 are analyzed and the corresponding waveforms are shown in Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19 respectively. This stress analysis illustrates that the switches are subjected to low voltage and current stresses compared to that for the conventional two-level boost converter. Hence, the switching losses are reduced in the proposed converter topology. The performance of the converter is validated by varying the duty ratio D of the switches from 0.6 to 0.9. The waveforms of voltages appearing across and the currents through the four diodes D_b, D_{br}, D_1, and D_2 are shown in Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, and Figure 27 respectively. The analysis of waveforms of diodes indicates that the diodes are also subjected to low voltage-current stress. The waveform of voltages appearing across the two identical capacitors C_1 and C_2 is illustrated in Figure 28. The voltages are balanced across the capacitors. The sum of these two capacitor voltages is obtained as the output voltage (V_0) at the load end. The charging and discharging current characteristics of the capacitors C_1 and C_2 are shown in Figure 29 and Figure 30 respectively.

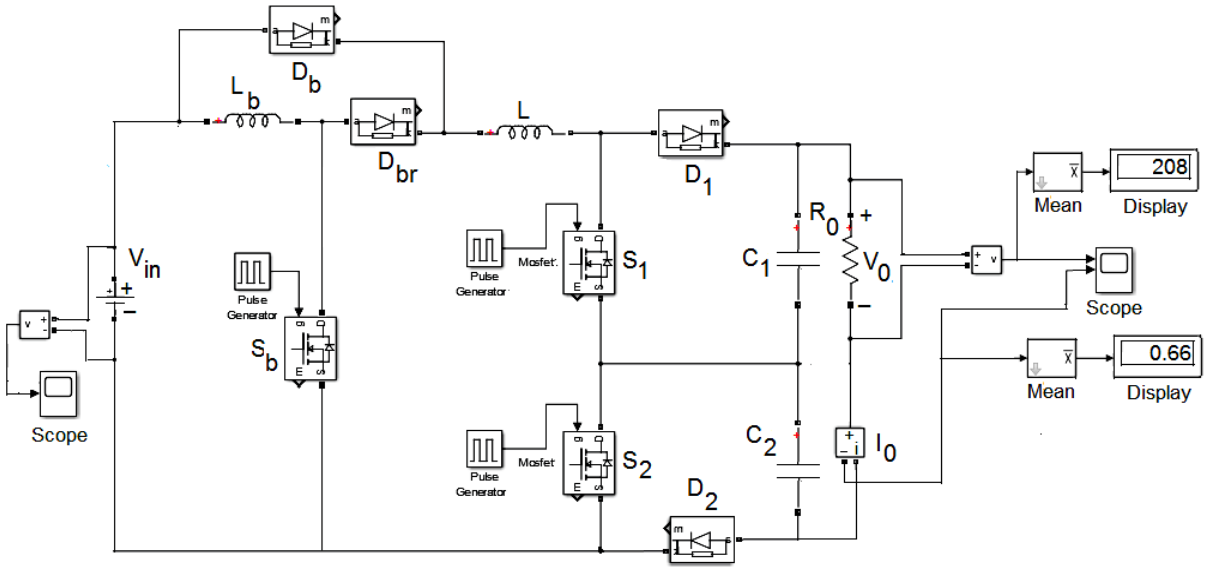


Figure 4. MATLAB / SIMULINK model of the proposed non-isolated DC-DC boost converter with boost power stage.

Table 1. Parameters of the proposed converter for simulation.

Parameters	Symbol	Value
Input DC voltage (V)	V_{in}	24
Output DC voltage (V)	V_0	208
Inductors (mH)	L_b, L	1 (each)
Capacitors (μF)	C_1, C_2	200 (each)
Switching frequency (kHz)	f_s	50
Load resistance (Ω)	R_0	311
Output DC current (A)	I_0	0.66
Duty ratio for each switch (S_b, S_1, S_2)	D	0.8

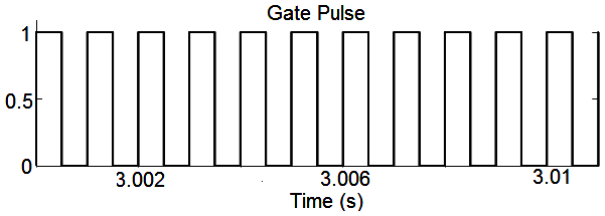


Figure 5. Gate pulse to the power switch.

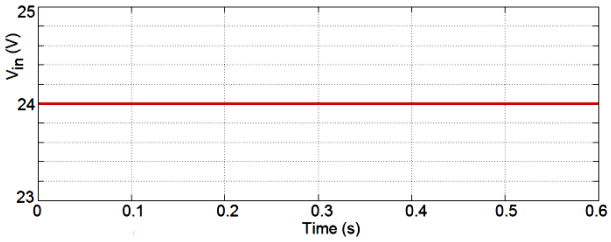


Figure 6. Input voltage.

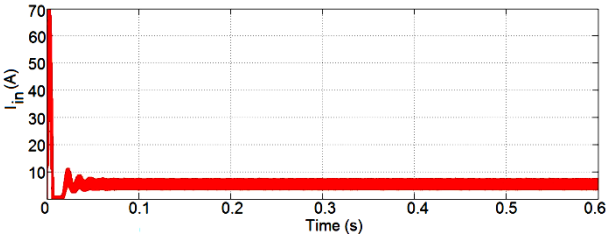


Figure 7. Input DC current.

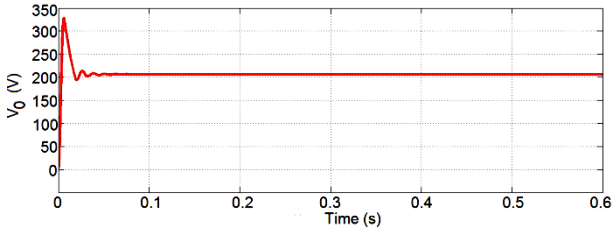


Figure 8. Output DC voltage across the load R_0.

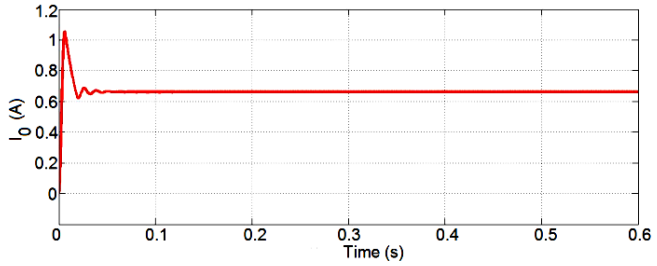


Figure 9. Output DC current through the load R_0.

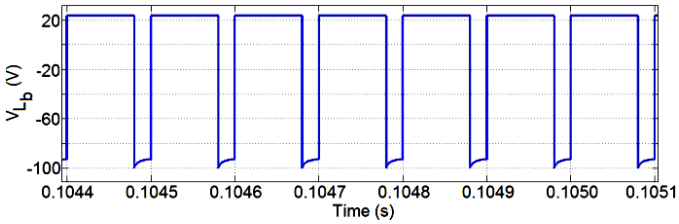


Figure 10. Voltage across the boost inductor L_b.

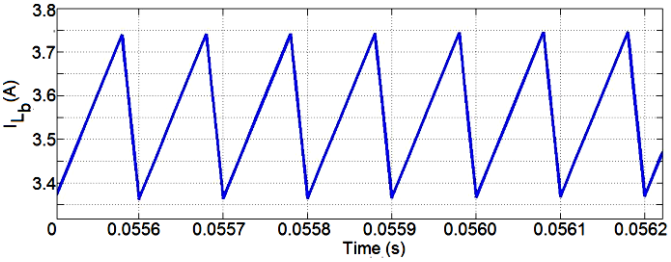


Figure 11. Current through the boost inductor L_b.

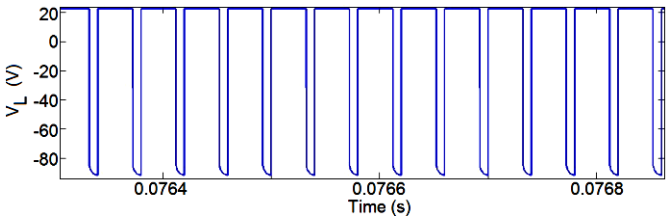


Figure 12. Voltage across the inductor L.

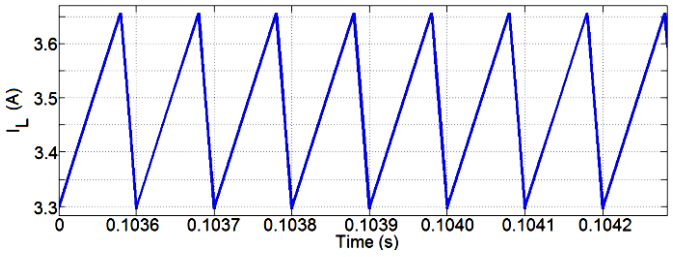


Figure 13. Current through the inductor L.

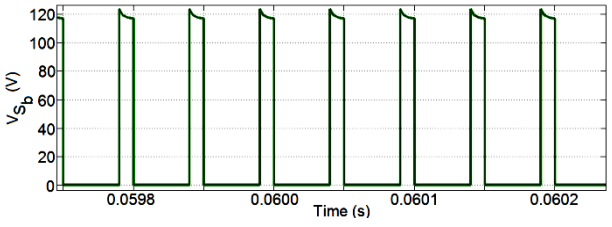


Figure 14. Voltage across the switch S_b.

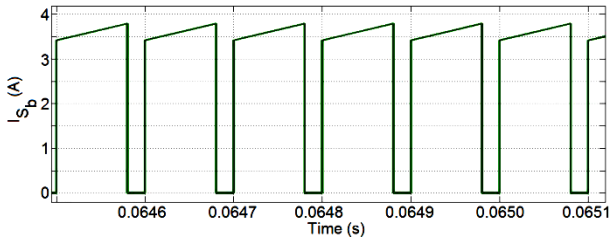


Figure 15. Current through the switch S_b.

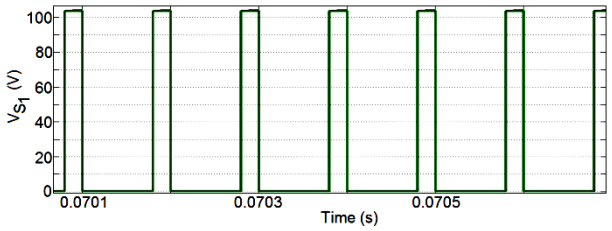


Figure 16. Voltage across the switch S_1.

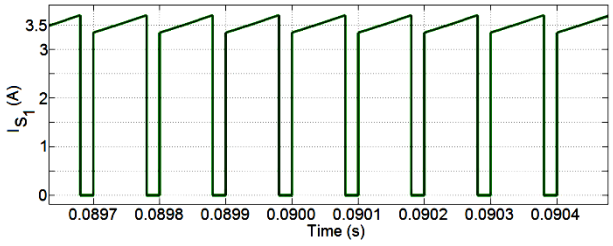


Figure 17. Current through the switch S_1.

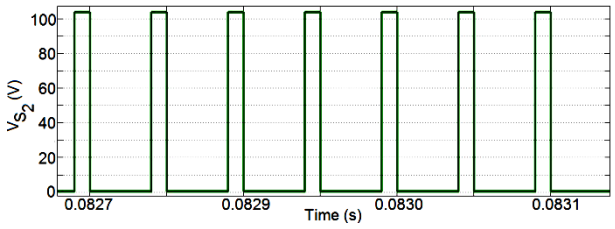


Figure 18. Voltage across the switch S_2.

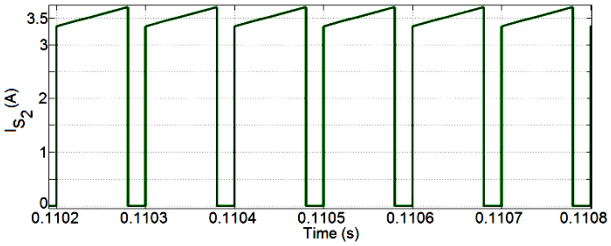


Figure 19. Current through the switch S_2.

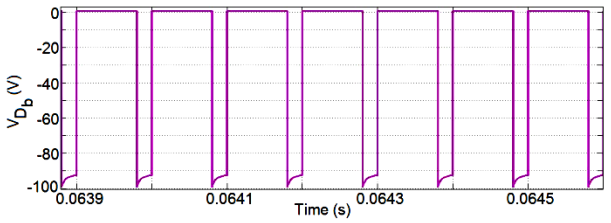


Figure 20. Voltage across the diode D_b.

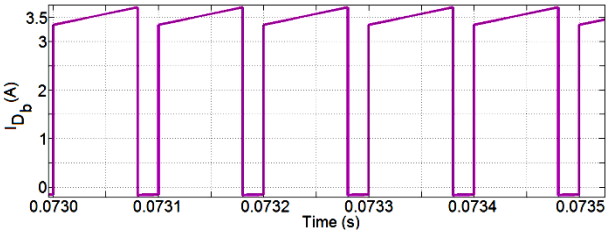


Figure 21. Current through the diode D_b.

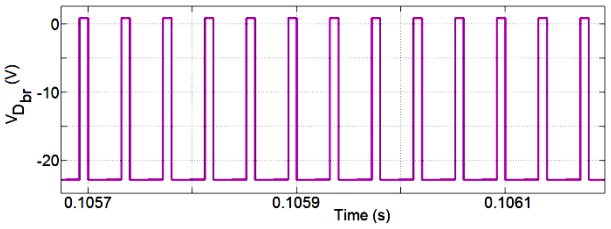


Figure 22. Voltage across the diode D_{br}.

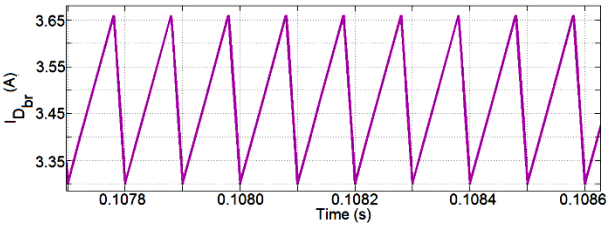


Figure 23. Current through the diode D_{br}.

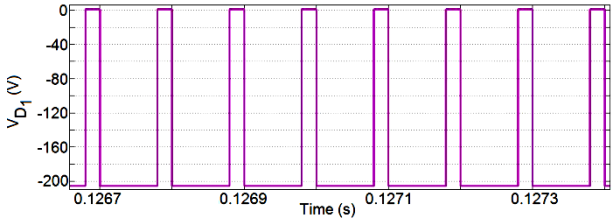


Figure 24. Voltage across the diode D_1.

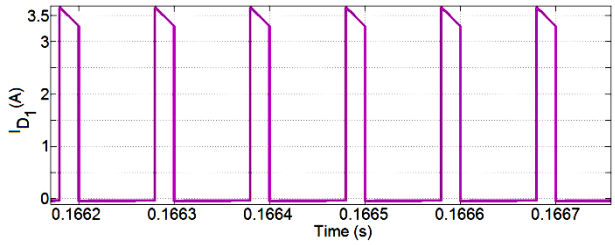


Figure 25. Current through the diode D_1.

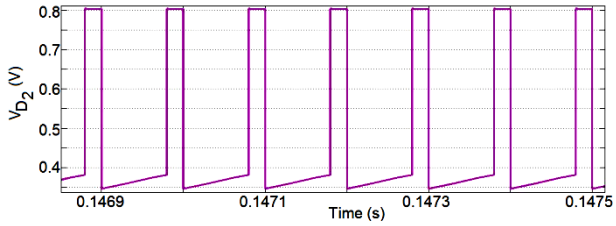


Figure 26. Voltage across the diode D_2.

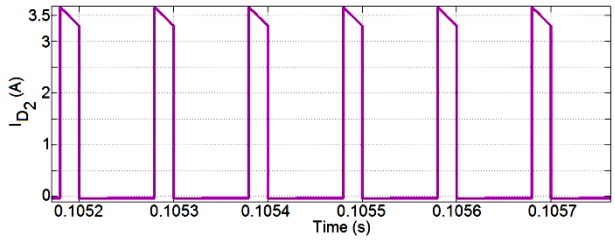


Figure 27. Current through the diode D_2.

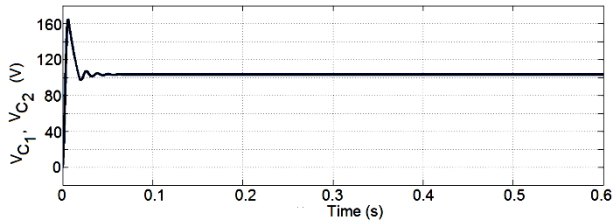


Figure 28. Voltage across the capacitors C_1 and C_2.

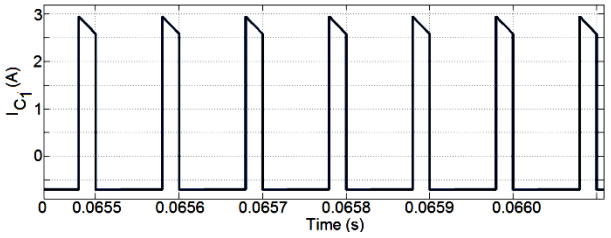


Figure 29. Current through the capacitor C_1.

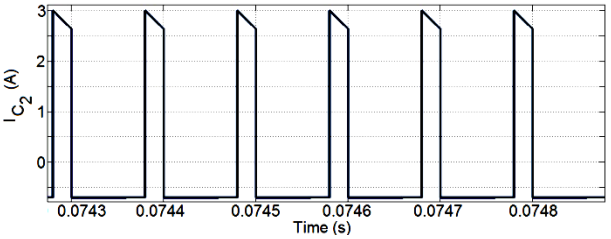


Figure 30. Current through the capacitor C_2.

4. Prototype model of the converter

The prototype model of a rectifier-fed DC-DC converter based on double boost topology capable to deliver 100 W output power has been developed and is as shown in Figure 31. The double boost topology includes all components of three-level configuration shown in Figure 1, except the switch S_2 and the capacitor C_2 (Liu et al., 2020). However, the voltage gain (G) equation is same for both the double boost topology and the three-level topology proposed in this work. The low power hardware model is designed to provide an output DC voltage of around 108 V at the load end for an average DC input voltage of around 12 V at the rectifier end. The power MOSFET switches are made to operate at duty ratio D = 0.8. The model employs an Integrated Circuit (IC) chip named as KA3525A PWM controller incorporating the control circuitry for the generation of pulse width modulated (PWM) signals for the MOSFET switches S_b and S_1. The PWM controller KA3525A is a 16 pin chip that requires a supply voltage of 40 V and features a reference output current of around 50 mA. It incorporates an error amplifier, voltage reference, a pulse width modulator, an undervoltage lockout, an oscillator, the output driver, and a soft start circuit, all in one package.

The power switches are turned ON and OFF simultaneously as per the gate pulse waveforms shown in Figure 32. The values of components of the hardware model of the converter are listed as shown in Table 2. The actual waveforms, taken on digital storage oscilloscope (DSO), for all internal components and power switches are shown in Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, Figure 38, Figure 39, Figure 40, Figure 41, and Figure 42 respectively.

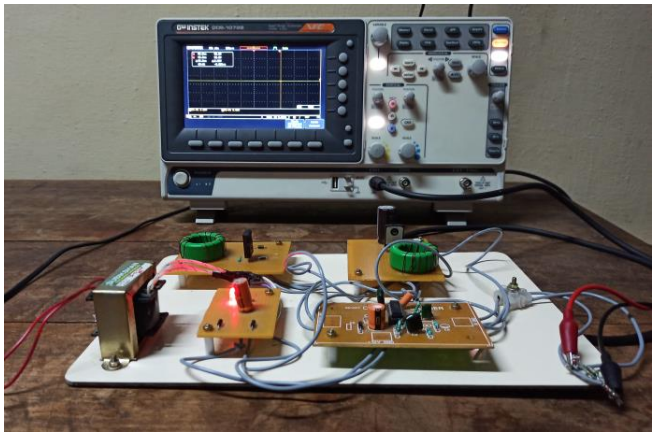


Figure 31. Prototype hardware model of the converter.

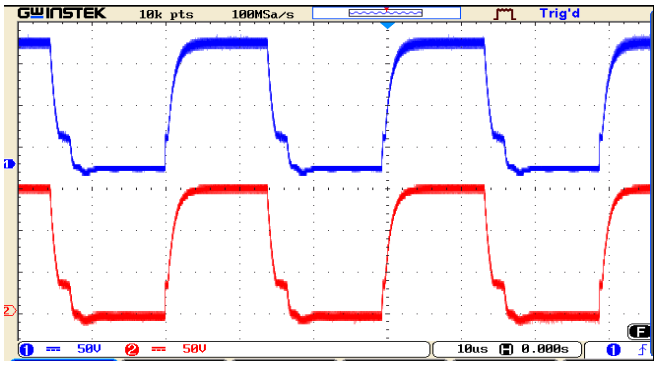


Figure 32. Gate pulse waveforms for the switches S_b and S_1.

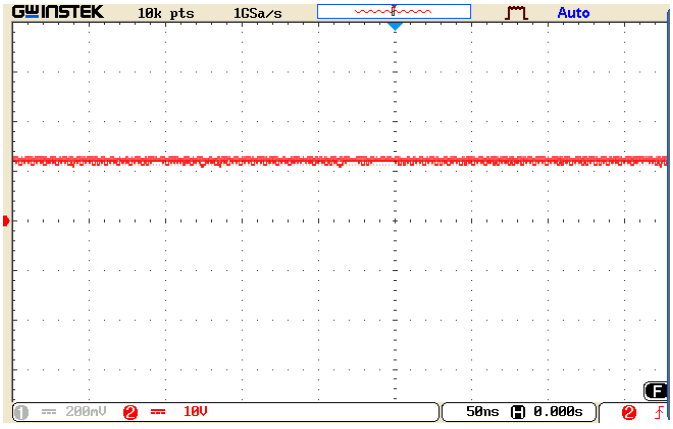


Figure 33. Average DC input voltage (V_{in}).

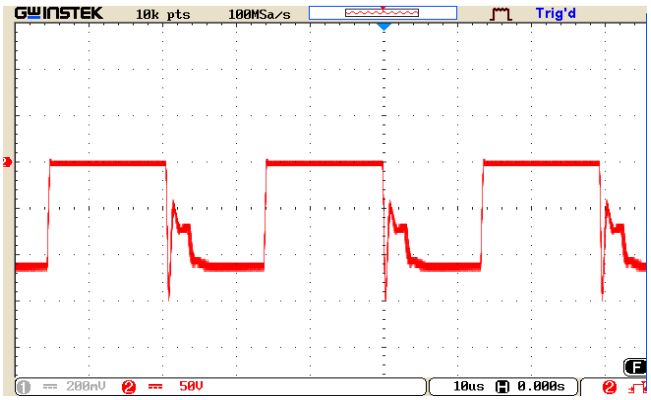


Figure 34. Voltage across the diode D_b.

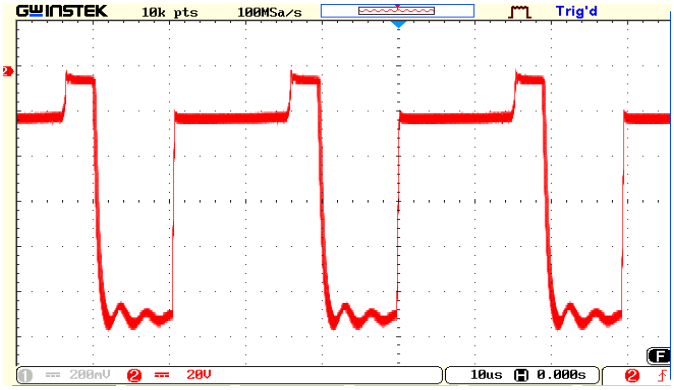


Figure 35. Voltage across the diode D_{br}.

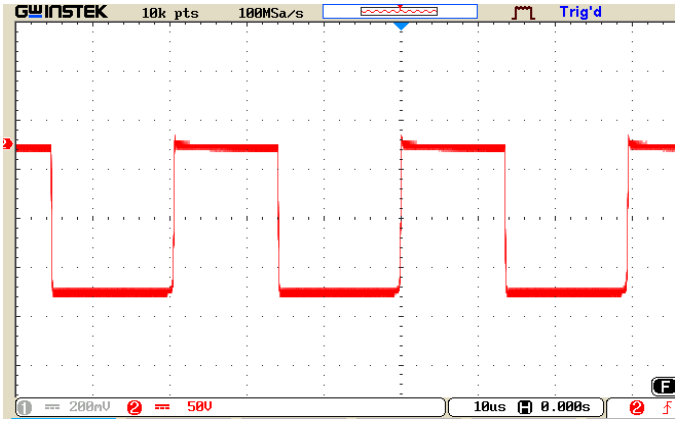


Figure 36. Voltage across the diode D_1.

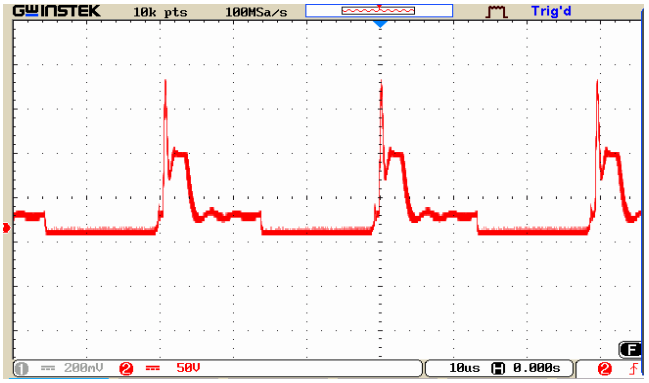


Figure 37. Voltage across the switch S_b.

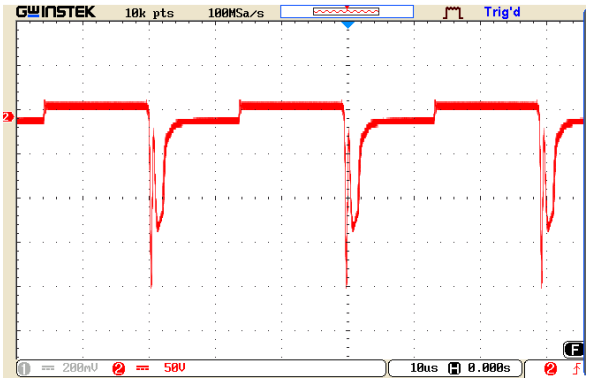


Figure 40. Voltage across the inductor L.

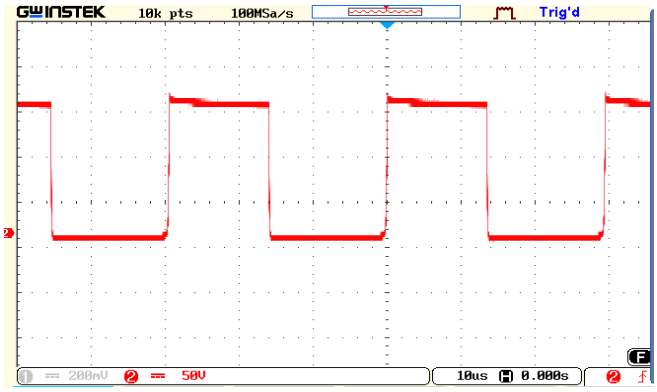


Figure 38. Voltage across the switch S_1.

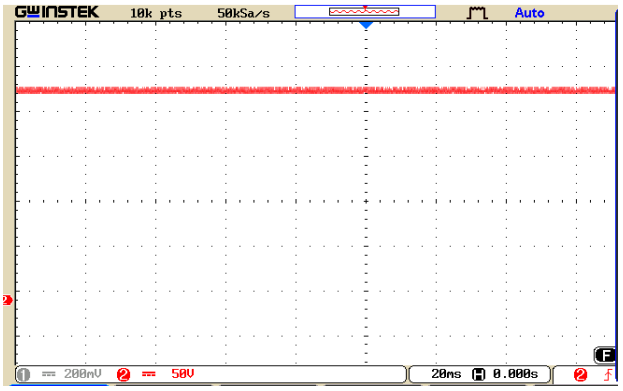


Figure 41. Output DC Voltage (V_0) equal to voltage across the capacitor C_1.

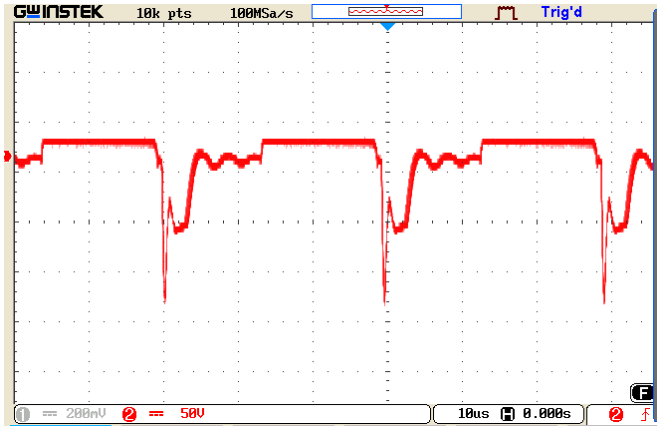


Figure 39. Voltage across the inductor L_b.

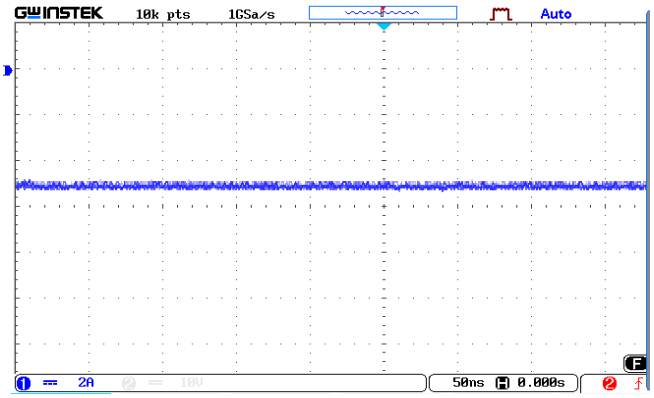


Figure 42. Output current (I_0).

Table 2. Components of the hardware model of the DC-DC converter.

Circuit components	Description	Type
S_b , S_1	Power MOSFETS	IFR640N, 200 V, 18 A
D_b, D_{br}, D_1	Diodes	DFE10I600PM, 600 V, 10 A
L_b, L	Inductors	0.35 mH each
C_1	Capacitor	47 µF
f_s	Switching frequency	30 kHz
R_0	Load resistance	100 Ω
P_0	Output power	100 W
I_0	Output current	1 A

5. Conclusions

In this paper, the steady state analysis of a non-isolated continuous input current positive output three-level DC-DC converter with boost power stage has been carried out. The validation of the performance of the proposed converter is done by simulating the converter in MATLAB / SIMULINK platform. The voltage and current waveforms for all the active and passive components of the converter are presented for duty ratio D = 0.8. The simulation results illustrate that the voltage gain of the proposed simple three-level DC-DC converter structure with boost power stage can be improved by (1+D) times that of the traditional three-level / boost configured DC-DC converter. The prototype model results are also provided to validate the theory and the time domain results. The additional features of the converter configuration proposed in this work are that the MOSFET switches are subjected to low voltage and current stresses thereby reducing the switching losses and hence improving the overall efficiency of DC-DC conversion. The diodes too experience low voltage-current stress. The filter components C_1 and C_2 are so chosen that the output voltage and current waveforms have only fewer amounts of ripples. Moreover, the output voltage and current waveforms settle down to steady state values after executing only few oscillations. The proposed converter is well-suited for renewable energy applications that require high voltage. Future work may include the application of the zero-voltage-switching concept to the active switches for switching loss reduction in the view to enhance the overall conversion efficiency.

Conflict of interest

The authors do not have any type of conflict of interest to declare.

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