



Parallel-charge series-discharge inductor-based voltage boosting technique applied to a rectifier-fed positive output DC-DC converter

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Received 03 20 2020; accepted 05 22 2020
Available online 10 31 2020

Abstract: The conventional power electronic boost converters have inherent limitations that they are not able to increase the low DC input voltage level into sufficiently high DC output voltage level. This is because of the fact that (1). the inductor used in the converter has certain amount of internal resistance, and (2). the power devices used in the converter are subjected to high potential stress which led to damage of the devices. A configuration of a non-isolated step-up rectifier-fed positive output power converter capable of converting low DC voltage into high DC output voltage-based on the concept of parallel-charge series-discharge inductors is proposed in this paper. The proposed converter is fed by an uncontrolled diode bridge rectifier to which an input sinusoidal AC voltage of magnitude 30 V (rms) is given. The converter is configured such that the input AC voltage of 30 V (rms) is stepped-up to around 900 V (DC) at the output of the converter, with extremely low duty ratio. The proposed converter configuration employs only two high power semiconductor switches with reduced complexity of control. In this work, the converter topology is presented, and its steady state behavior and dynamic modeling are discussed for continuous inductor current mode operation. Further, it is revealed that the voltage gain of the converter is influenced by the variation of the duty cycle of the power switches. The effectiveness of the converter is better understood through simulation in MATLAB/SIMULINK platform. The results demonstrate that the converter is able to maintain higher constant output voltage profile with significantly reduced overshoot and settling time.

Keywords: Continuous inductor current mode, Discontinuous inductor current mode, Duty cycle, Dynamic modeling, MATLAB/SIMULINK, Parallel-charge series-discharge inductors, Positive output power converter, Steady state modeling, Voltage gain.

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Peer Review under the responsibility of Universidad Nacional Autónoma de México.

1. Introduction

In recent advancements, DC-DC power electronic boost converters have had a significant role in various applications such as hybrid electric vehicles, fuel cell energy conversion systems, medical equipment, military applications, battery charging and many more, where the high DC output voltage is obtained with the high ON time of the power switches. However, the high ON time (high duty cycle) led to certain issues such as reduced efficiency of power conversion, high potential stress across the switches, severe reverse-recovery issue of diodes, and electromagnetic interference problems (Hsieh, Chen, Liang, & Yang, 2012; Yang, Liang, & Chen, 2009). The conventional boost converters may be cascaded to increase the DC output voltage level with low value duty cycle operation (Prabhala, Fajri, Gouribhatla, Baddipadiga, & Ferdowsi, 2016; Wai, Lin, Duan, & Chang, 2007). While cascading, the efficiency of power conversion gets decreased. Another disadvantage is that the increased potential stress appearing across the power switch and the diode at the output stage. A single switch-based concept of cascading two boost converters was used in the quadratic converter. But this type of converter employed inductor and capacitor of higher ratings and suffers from the high potential switch stress. Several stacked converters are introduced by some authors to increase the voltage gain (Dwari & Parsa, 2011; Wu, Chen, Yang, & Kuo, 2010). However, these types of converters also suffer from the disadvantage that the capacitors at the output need to maintain voltage balance across them particularly when their number is increased. The voltage stress appearing across the output diode of the conventional boost converter can be mitigated using three levels in the conventional converter and the increase in effective frequency can reduce the size of inductors (Yaramasu & Wu, 2011). This converter is impracticable for certain applications due to the insufficient voltage level at the output.

There are certain types of isolated power electronic converters which utilize the concept of adjusting the number of turns on the primary and secondary side of the transformer to obtain the increased output voltage levels. However, the high leakage inductance of the transformer and increased potential switch stress limit the applications of these converters. Some authors developed certain converter configurations that are able to produce high DC output voltage, high power conversion efficiency and reduced switch stress by utilizing magnetically coupled inductor along with transformer (Duarte et al., 2013; Evran & Aydemir, 2014; Forouzesh, Siwakoti, Gorji, Blaabjerg, & Lehman, 2017; Tofoli, de Castro Pereira, de Paula, & Júnior, 2015). But many converter topologies that can improve both the voltage gain

and efficiency are presented in the literature (Chub, Vinnikov, Blaabjerg, & Peng, 2016; He & Khaligh, 2017; Hu & Gong, 2014; Tseng & Huang, 2014).

It is also possible to reduce the switch stress along with improved output voltage level if voltage multiplier cells are hybridized with the conventional single switch power converters. The conventional, Cuk and SEPIC DC-DC converters employ voltage multiplier circuitry (Chub et al., 2016). The conventional step-up converter's gain may be increased N times by a power electronic converter which is capable to produce inverting DC output voltage (Mahajan, Sanjeevikumar, Ojo, Rivera, & Kulkarni, 2016). Further, there are power converters that employ interleaved boost concept to increase the DC output voltage level with reduced ripples in the output voltage and output current (Bhaskar, Kulkarni, Padmanaban, Siano, & Blaabjerg, 2016). Some authors proposed the concept of interleaved multilevel voltage multiplier-based power converter topologies that are capable to produce $2N$ and $4N$ times the output voltage level of conventional boost topology (Bhaskar, Sanjeevikumar, et al., 2016). But, this high output voltage level is influenced by (i). balancing of voltages across the various capacitors with suitable time constants, and (ii). more number of diodes. The charge and discharge characteristics of the capacitors influence the power conversion efficiency (Bhaskar, et al., 2016). Two or more conventional boost converters can be connected in parallel using interleaving technique. This interleaving technology can easily cause the filtering of ripples in the input current (Li & He, 2011; O'Loughlin, 2006; Roy & Ayyanar, 2017). The range of DC output voltage can be increased using coupled inductors along with voltage multiplier units (Rosas-Caro et al., 2011). However, while using coupled inductors concept, energy circulation and snubber circuits are required to reduce the potential stress across the switches.

Switched capacitor (SC)-based converters, having high efficiency with good output voltage regulation and low weight, mainly consist of large number of switching devices and capacitors with various ratings, and the output voltage level can be boosted by the charge and discharge characteristics of capacitors (Mahajan, Sanjeevikumar, & Blaabjerg, 2017; Qian et al., 2012). The use of large number of switching devices leads to high switching losses. Hence, the efficiency of the SC-based DC-DC converter cannot be improved due to large power rating of the switching devices. Moreover, the increase of voltage gain of the converter is also limited. The SC-based converter circuits can have higher energy and power densities since they do not use reactive elements for energy transfer. Moreover, the SC circuit can be fabricated into an integrated chip (IC) and mostly used in low-power electronics applications.

There is another possible solution for improving the DC voltage gain of the converter using switched inductor (SI)-based DC-DC conversion technology, which employs parallel-charge and series-discharge inductors (Yang et al., 2009; Gautam, Sharma, & Shukla, 2019). This switched inductor-based converter configuration can operate in boost mode as well as in buck-boost mode. When it is operated in boost mode, then the configuration is called switched inductor boost converter (SI-BC), and in buck-boost mode, it is called switched inductor buck boost converter (SI-BBC). These configurations employ only a single active switch. But the switch is subjected to high voltage stress. Both the SI-BC and SI-BBC configurations are capable to improve the voltage gain by (1+Duty ratio) times and two times compared to the respective conventional DC-DC converters.

Some authors proposed a high step-up DC-DC converter structure consisting of a full-bridge module and the Cockcroft-Walton principle-based voltage multiplier to achieve high voltage gain in photovoltaic applications (Hossain, Selvaraj, & Rahim, 2018). A quasi-switched boost inverter configuration with voltage multiplier cell can be used for achieving high voltage gain with decreased voltage stress on the switches (Nguyen & Chai, 2019). A non-isolated approach of LLC resonant DC-DC converter with balanced rectifying current and stress has been proposed by some authors (Dobi & Sahid, 2020). This configuration has significantly reduced transformer loss because of non-isolation. The PI controller-based super lift technique applied to DC-DC Luo converters has been proposed by some authors to improve the voltage conversion ratio (Adlakha, Khosla, & Joshi, 2020) in which the comparative analysis of various positive output super lift DC-DC Luo converters is discussed. A non-isolated high voltage gain DC-DC converter proposed in (Saravanan & Ramesh Babu, 2019) is compared with boost, SEPIC and modified SEPIC converters. The converter proposed in (Saravanan et al., 2019) shows high efficiency compared to the other converters.

In this work, a diode rectifier-fed positive output power electronic converter, capable to increase the DC output voltage to the higher level without using high duty ratio of the switches, is analyzed theoretically and using simulation software. Here, three identical inductors each of value 0.1 mH are used. The concept of parallel-charge and series-discharge characteristics of the switched inductors is used to increase the DC output voltage level to the higher value. It employs only two power semiconductor switches which are subjected to

low voltage and current stresses during the switch-off and switch-on periods. There are certain assumptions to be made for the analysis of the proposed converter:

- 1). The diodes and MOSFETs used in the converter have negligible forward voltage drops and are having negligible resistance during forward conduction mode. The inductors and capacitors used are lossless.
- 2). Large capacitances are assumed for the capacitors to maintain constant voltages across them.
- 3). The current flow through the three inductors in the proposed configuration increases or decreases linearly.

The remaining sections are arranged in such a way that the proposed work is illustrated effectively. The section 2 describes the configuration and various modes of operation of the converter under study. The MATLAB / SIMULINK model of the converter and its time domain simulation results are discussed in section 3. The conclusion for the proposed work is given in section 4.

2. Configuration and modes of operation of the converter under study

The topology of a rectifier-fed non-isolated high step-up positive output converter capable of producing high DC output voltage is shown in Figure 1. The single-phase AC supply of 50 Hz frequency is fed to a diode bridge rectifier which gives an uncontrolled DC voltage. The ripples in the DC voltage are filtered by a capacitor. The filtered DC output voltage is acting as source to the DC-DC converter stage whose output is filtered by a capacitor C_0 . The converter output voltage appears across a load R_L . The proposed converter employs three identical inductors of inductances L_1 , L_2 and L_3 respectively. The two high power semiconductor switches S_1 and S_2 are triggered simultaneously into conduction by proper gate signals. The theoretical waveforms of the rectifier-fed converter operating under continuous and discontinuous inductor currents are presented in Figure 2. Both the continuous and discontinuous modes of operations of the converter are discussed. In this work, the simulation of the proposed converter is carried out under continuous inductor current mode. The various modes of operation of the converter under continuous and discontinuous inductor current modes are explained as shown below:

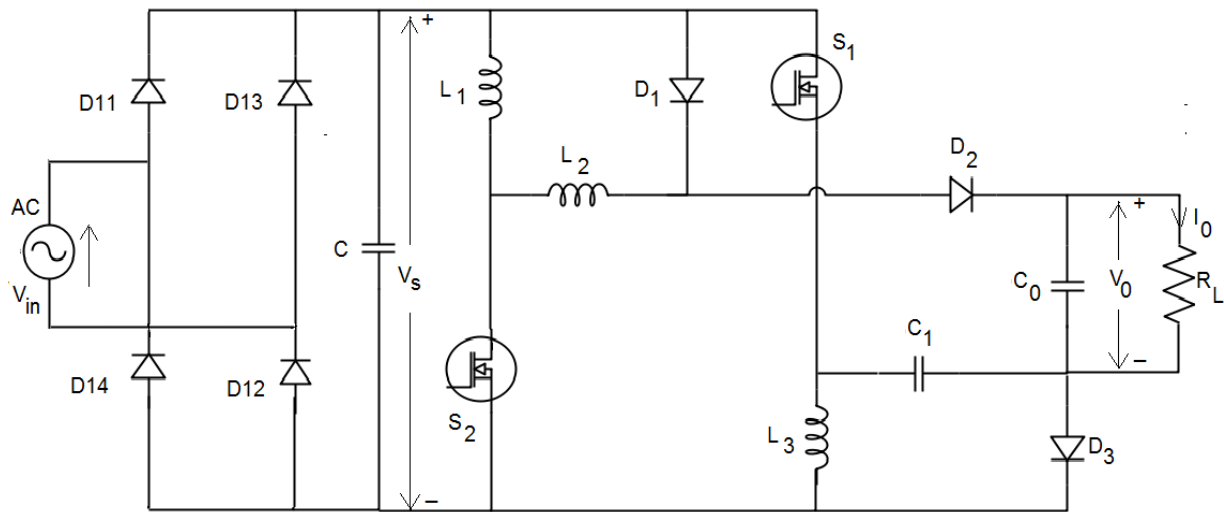


Figure 1. Circuit configuration of the proposed rectifier-fed non-isolated positive output DC-DC boost converter.

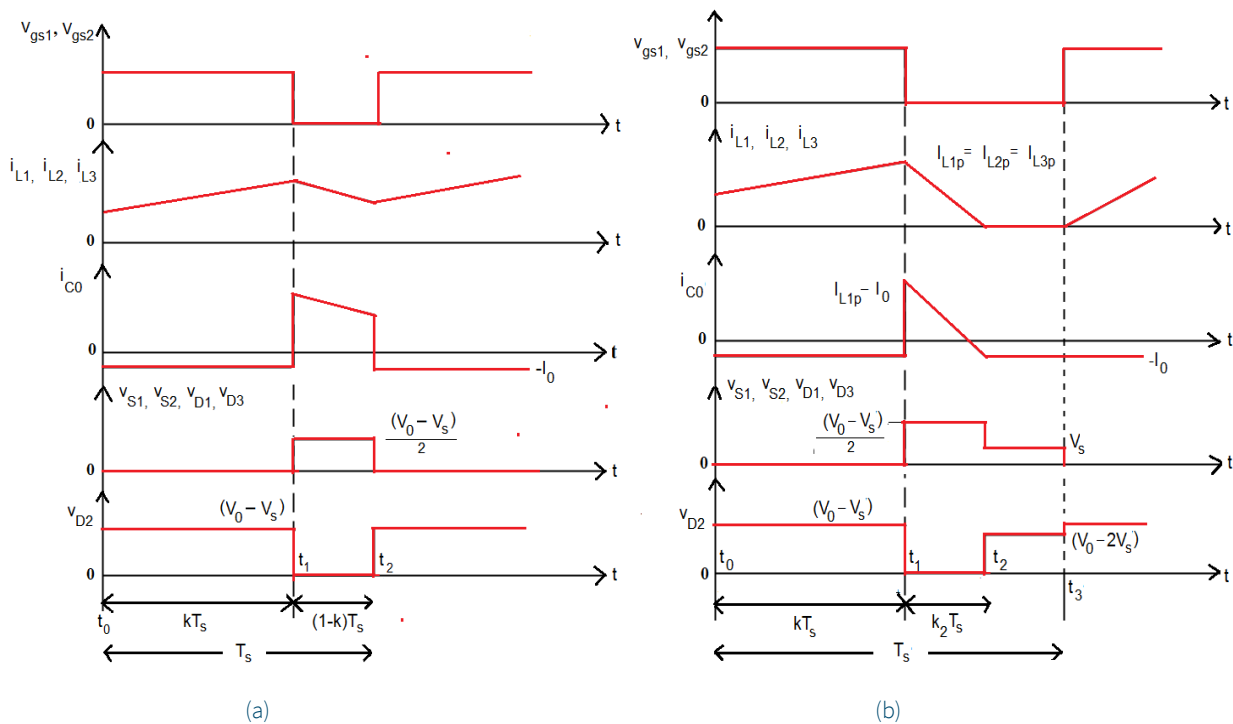


Figure 2. Theoretical waveforms of the converter under study during (a). continuous inductor current mode, and (b). discontinuous inductor current mode.

2.1. Mode-I operation of the converter during the time interval $t_0 - t_1$

2.1.1. Steady-state analysis:

Both the high power semiconductor switches S_1 and S_2 , of the converter under continuous inductor current mode / discontinuous inductor current mode, are switched on during the time interval $t_0 - t_1$. This mode of operation of the converter is represented in Figure 3. The diodes D_1 and D_3 get forward-biased. The diode D_2 gets reverse-biased. The average rectified DC output voltage V_s charges all the three identical inductors in parallel, and the load resistor R_L receives the energy from the capacitor C_0 . The diodes and MOSFETs used in this work are assumed as ideal devices having negligible forward voltage drops due to negligible resistance during forward conduction mode. All three inductor currents will be equal since the three inductors are identical and are connected across V_s during mode-I operation as shown in Figure 3. The capacitor C_1 also gets charged from the source V_s .

Thus, the three identical inductors and the capacitor C_1 are charged in parallel to the source voltage V_s .

$$v_{L1} = v_{L2} = v_{L3} = V_{C1} = V_s \tag{1}$$

2.1.2. State-space analysis:

The dynamic and output equations of the circuit for the ON period of the switches S_1 and S_2 are obtained as follows:

By applying Kirchoff's Voltage Law to the circuit shown in Figure 3, we get

$$V_s = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = L_3 \frac{di_{L3}}{dt} \tag{2}$$

Since all the three identical inductors carry equal currents, $L_1 = L_2 = L_3 = L \quad i_{L1} = i_{L2} = i_{L3} = i_L$

$$\text{Eqn.(2) can be written as: } V_s = L \frac{di_L}{dt} \tag{2.a}$$

$$\frac{di_L}{dt} = \frac{V_s}{L} \tag{2.b}$$

By applying Kirchoff's Current Law to the circuit shown in Figure 3, we get

$$0 = \frac{v_{C0}}{R} + C_0 \frac{dv_{C0}}{dt} \tag{3}$$

$$\frac{dv_{C0}}{dt} = -\frac{v_{C0}}{RC_0} \tag{3.a}$$

From Eqns (2.b) and (3.a), the state-space model of the proposed converter during ON period is written as Eqns. (4.a) and (4.b):

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{C0}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC_0} \end{bmatrix} \begin{bmatrix} i_L \\ v_{C0} \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} V_s \tag{4.a}$$

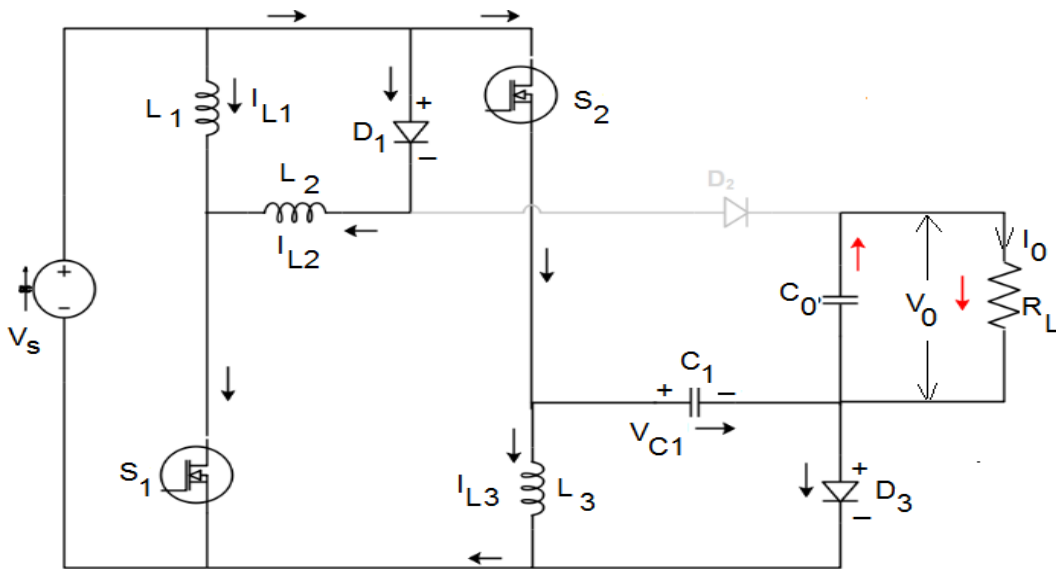


Figure 3. Circuit representation of the converter during Mode-I operation.

$$v_0 = [0 \quad 1] \begin{bmatrix} i_L \\ v_{C0} \end{bmatrix} \quad (4.b)$$

2.2. Mode-II operation of the converter during the time interval $t_1 - t_2$:

2.2.1 Steady-state analysis:

Both the high power semiconductor switches S_1 and S_2 , of the converter under continuous inductor current mode / discontinuous inductor current mode, are turned-off during the time interval $t_1 - t_2$. This mode of operation of the converter is represented in Figure 4. The diode D_2 gets biased in the forward direction. The diodes D_1 and D_3 get biased in the reverse direction. During mode-I, the diode D_1 was forward biased. Therefore, the current flow through L_2 will be as shown in Figure 3. Whereas during mode-II, the diode D_1 gets reverse biased. Hence, the diode D_1 gets open circuited and the diode D_2 gets forward biased. Therefore, the current flow through L_2 during mode-II in Figure 4 will be opposite to that during mode-I shown in Figure 3. All the three identical inductors and the capacitor C_1 are connected in series with the average DC voltage source V_s to transfer the energies to the capacitor C_0 and the load resistor R_L . However, the current through the inductors are decreased to zero at the end of the interval ($t = t_2$) during discontinuous inductor current mode. Under continuous inductor current mode of the converter during mode-II, the voltages across the inductors are obtained as (Yang et al., 2009):

$$V_s + v_{L2} + V_{C1} = V_0 + v_{L1} + v_{L3} \quad (5)$$

From the Figure 4, it is understood that all the three identical inductors carry the same current. Hence, they have the equal voltage drop of V_s across them.

$$V_s + V_s = V_0 + 2v_{L1} - v_{L1}$$

$$2V_s = V_0 + v_{L1}$$

Therefore, $v_{L1} = v_{L2} = v_{L3} = 2V_s - V_0$ (6)

The Inductor Volt-Second Balance (IVSB) principle states that for steady state operation of an inductor in a DC-DC converter, the net inductor voltage in a switching period must be zero. By referring Figure 2, the following Eqn. (7) is obtained by applying the IVSB principle on the inductors L_1 , L_2 and L_3 :

$$\int_0^{kT_s} V_s dt + \int_{kT_s}^{T_s} (2V_s - V_0) dt = 0 \quad (7)$$

$$V_s kT_s + (2V_s - V_0)(T_s - kT_s) = 0$$

$$V_s(k + 2 - 2k) = V_0(1 - k)$$

Finally, the voltage gain G_c under continuous inductor current mode operation of the converter with the active switches having duty ratio k is obtained as:

$$G_c = \frac{V_0}{V_s} = \frac{2-k}{1-k} \quad (8)$$

2.2.2. State-space analysis:

The dynamic and output equations of the circuit for the OFF period of the switches S_1 and S_2 are obtained as follows:

By applying Kirchoff's Voltage Law to the circuit shown in Figure 4, we get

$$V_s - v_{C0} = (L_1 + L_2) \frac{di_{L1}}{dt} = 2L \frac{di_L}{dt} \quad (9.a)$$

$$\frac{di_L}{dt} = \frac{1}{2L} V_s - \frac{1}{2L} v_{C0} \quad (9.b)$$

By applying Kirchoff's Current Law to the circuit shown in Figure. 4, we get

$$i_{L1} = i_{L2} = i_L = \frac{v_{C0}}{R} + C_0 \frac{dv_{C0}}{dt} \quad (10.a)$$

$$\frac{dv_{C0}}{dt} = \frac{1}{C_0} i_L - \frac{1}{RC_0} v_{C0} \quad (10.b)$$

From Eqns (9.b) and (10.b), the state-space model of the proposed converter during OFF period is written as Eqns. (11.a) and (11.b):

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{C0}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L} \\ \frac{1}{C_0} & -\frac{1}{RC_0} \end{bmatrix} \begin{bmatrix} i_L \\ v_{C0} \end{bmatrix} + \begin{bmatrix} 1/(2L) \\ 0 \end{bmatrix} V_s \quad (11.a)$$

$$v_0 = [0 \quad 1] \begin{bmatrix} i_L \\ v_{C0} \end{bmatrix} \quad (11.b)$$

2.3. Mode-III operation of the converter during the time interval $t_2 - t_3$:

Both the active switches S_1 and S_2 of the converter under discontinuous inductor current mode are still switched-off during the time interval $t_2 - t_3$. This mode is represented in Figure 5. All the three diodes are not conducting. The three inductors have no stored energy. Thus, the load R_L receives the power delivered by the capacitor C_0 .

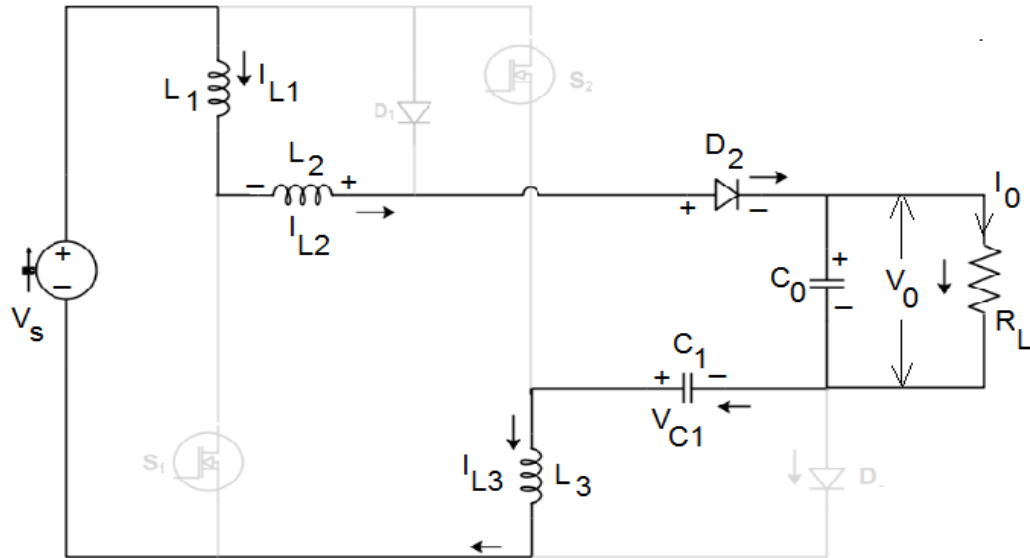


Figure 4. Circuit representation of the converter during Mode-II operation.

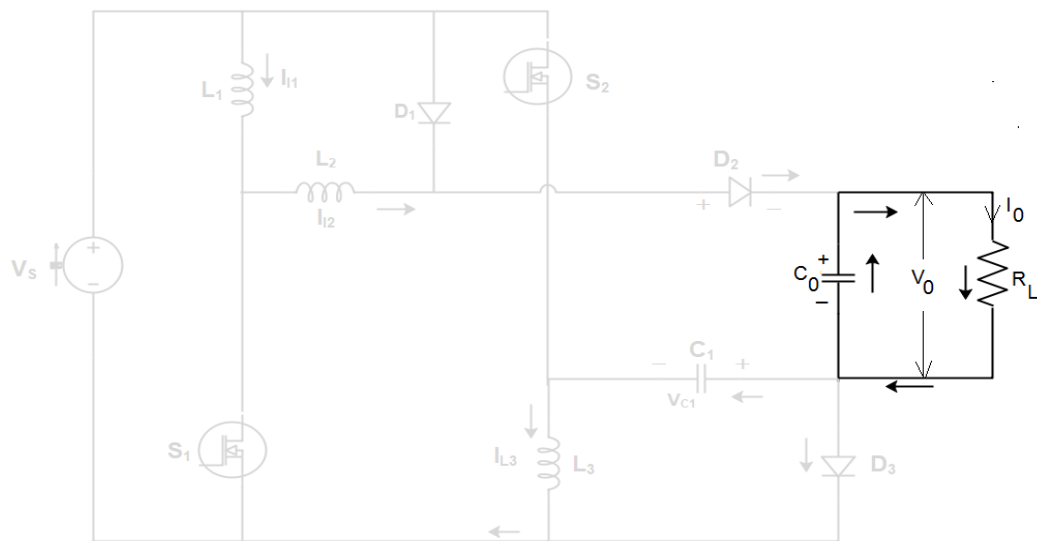


Figure 5. Circuit representation of the converter during Mode-III (Discontinuous inductor current mode) operation.

3. MATLAB / SIMULINK model of the converter under study and its time-domain simulation results

The Simulink model of the rectifier-fed non-isolated positive output converter is developed as shown in Figure 6 and the converter operating under continuous inductor current mode is simulated in Matlab/Simulink environment at a switching frequency of 3 kHz. Table 1 lists the values of circuit components used for simulation. Table 1 also lists the specifications of the converter under study. The converter circuit is simulated using solver 'ode 45' of variable-step type. A graphical user interface (GUI) is utilized by the simulink for solving process related simulations. The gating signals given to the active switches S_1 and S_2 are indicated in Figure 7. The duty ratio ' k ' of the switches is varied between 0.5 and 0.9. But, at extremely low duty ratio ($k = 0.6$) itself, high voltage conversion ratio is obtained. The waveforms of input AC voltage, load voltage and load current are indicated in Figure 8 and Figure 9 respectively. The currents through the three identical inductors are shown in Figure 10. The waveforms of

voltages across the three inductors are shown in Figure 11. The waveforms of voltages across and the currents through the capacitors C_0 and C_1 are shown in Figure 12 and Figure 13 respectively. The capacitor C_1 has sudden variation of voltage across it due to the change of direction of current through it when the mode of operation changes from I to II. The voltage stresses across the switches are indicated in Figure 14. The waveforms of current through the switches are shown in Figure 15. Figure 16 shows the waveforms of voltages appearing across the diodes D_1 , D_2 and D_3 . The waveforms of the currents through the diodes are shown in Figure 17. An AC input voltage of 30 V (rms) is given as input to the diode rectifier. At the end of the rectifier, an average DC output voltage of around 90 V is obtained. The output voltage across the load for the duty ratio $k = 0.6$ is almost 900 V (DC), which is almost 10 times the average DC voltage obtained at the output of the rectifier. The load current is of the order of 0.2 A. The active switches are subjected to the voltage stress of around 83 V only. The active switch stresses are reduced as the duty ratio ' k ' of the switches increases.

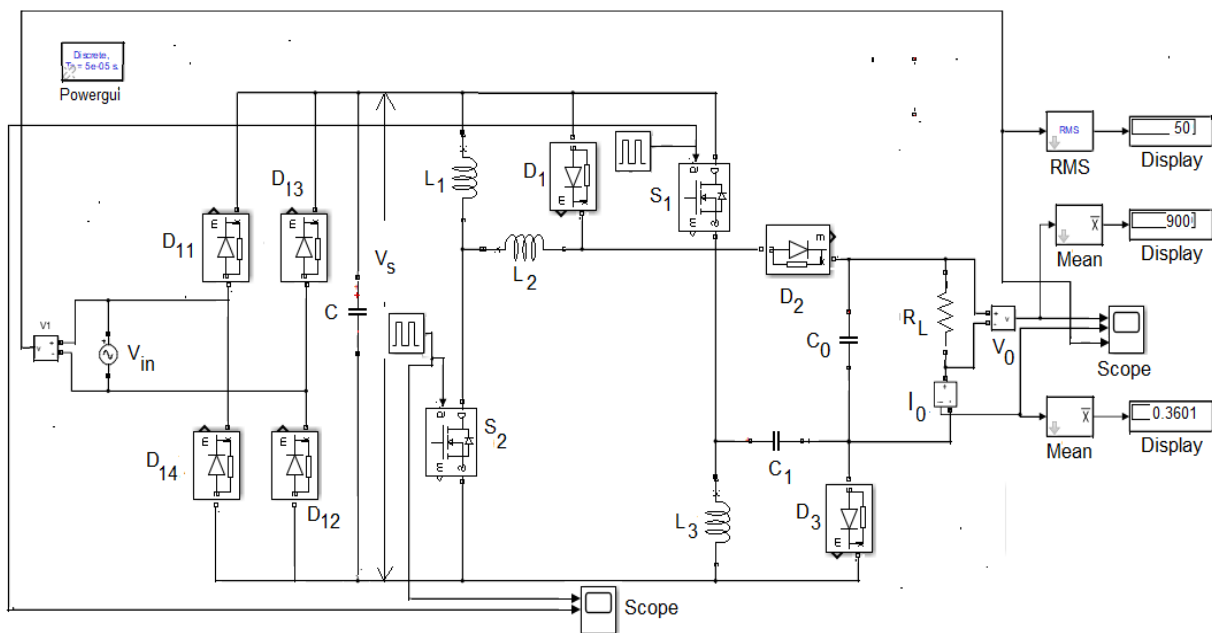


Figure 6. Simulation diagram of the proposed rectifier-fed DC-DC converter configuration

Table 1. Simulation parameters of the proposed converter.

Parameters	Symbol	Value
Input Voltage	V_{in}	30 V (rms)
Rectifier output voltage	V_s	90 V (Average DC)
Output Voltage	V_o	900 V (DC)
Inductors	L_1, L_2, L_3	0.1 mH each
Capacitors	C, C_1, C_0	100 μ F, 360 μ F, 280 μ F
Switching frequency	F_s	3 kHz
Load Resistance	R_L	5 kW
Load power	P_o	160 W
Average output current	i_o	0.18 A
Duty ratio of the switches	k	0.6

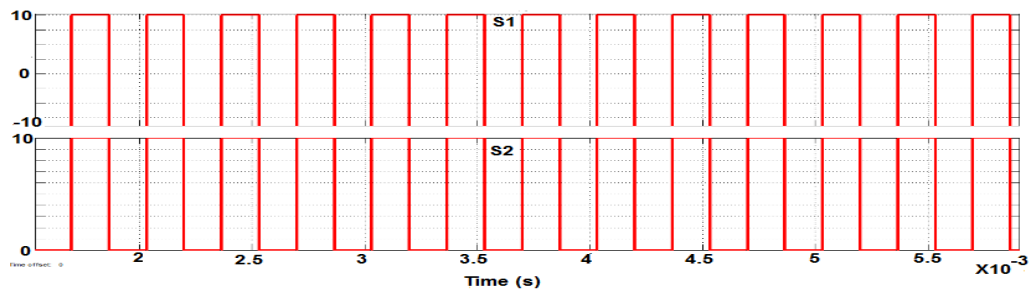


Figure 7. Gating pulses to the switches S_1 and S_2 .

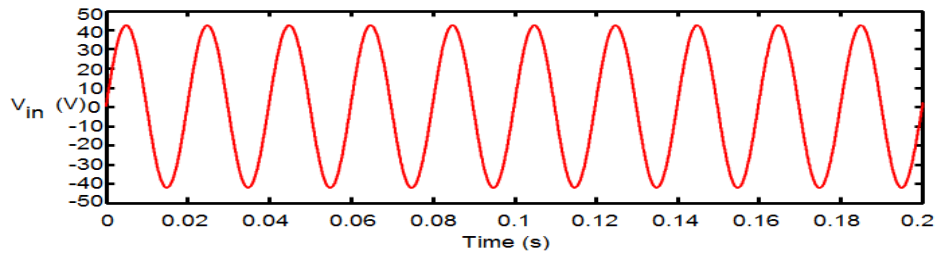


Figure 8. Input AC voltage (V_{in}) waveform as a function of time.

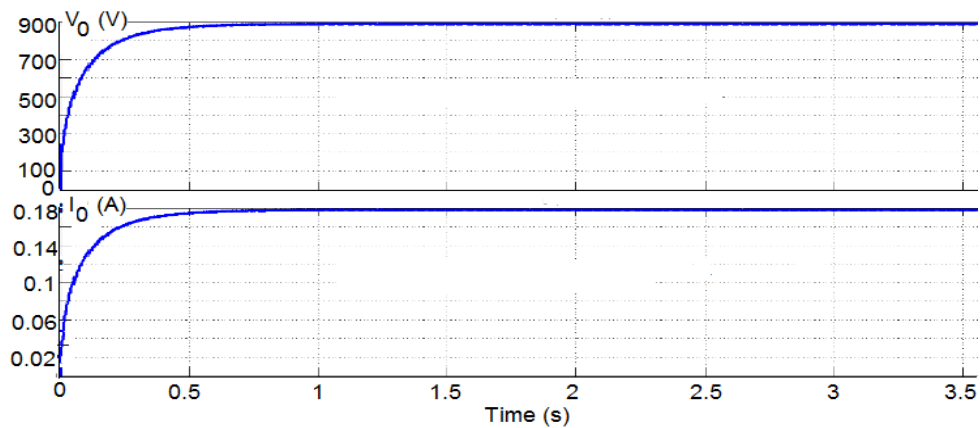


Figure 9. Output voltage and output current waveforms.

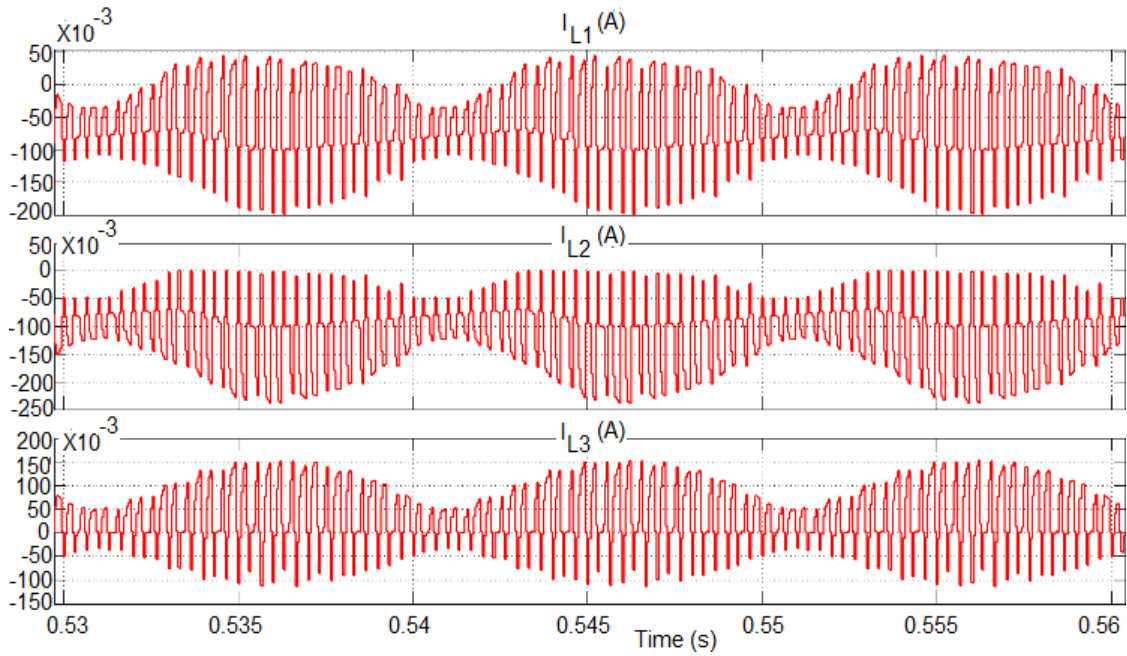


Figure 10. Currents through inductors L1, L2, and L3.

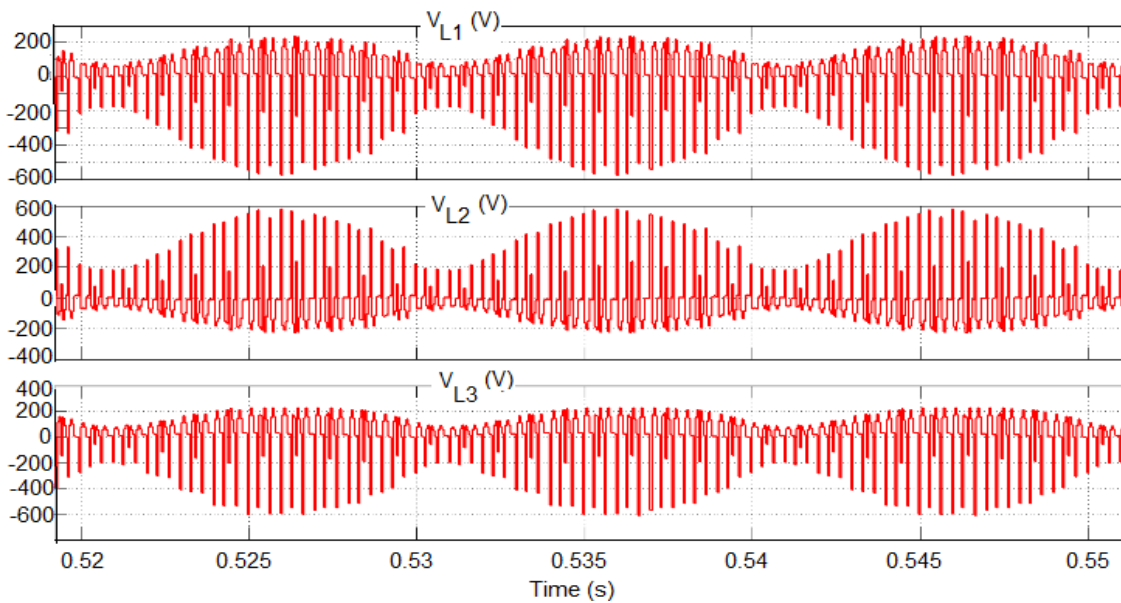


Figure 11. Voltages across the inductors L1, L2, and L3.

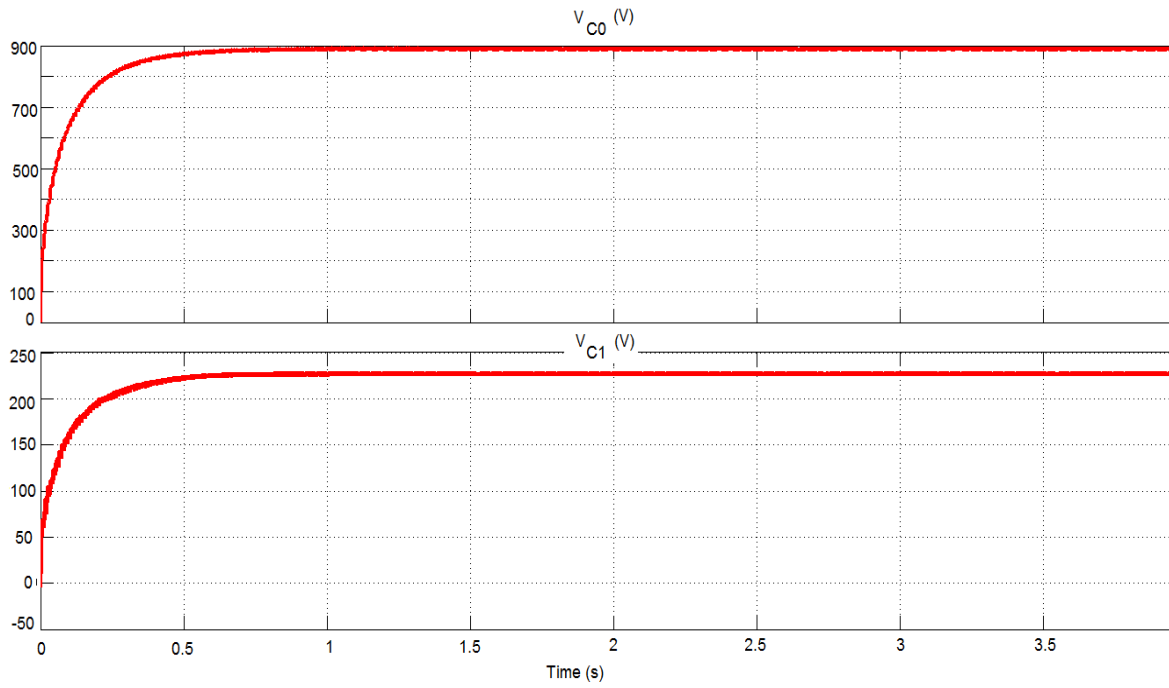


Figure 12. Voltages across the capacitors C_0 and C_1 .

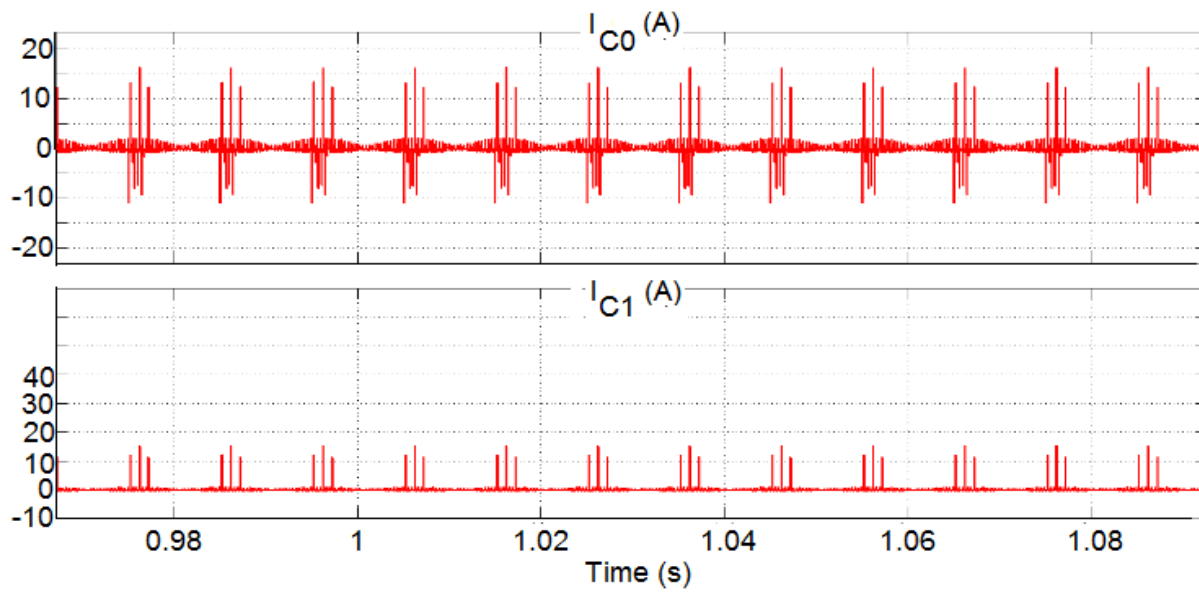


Figure 13. Currents through the capacitors C_0 and C_1 .

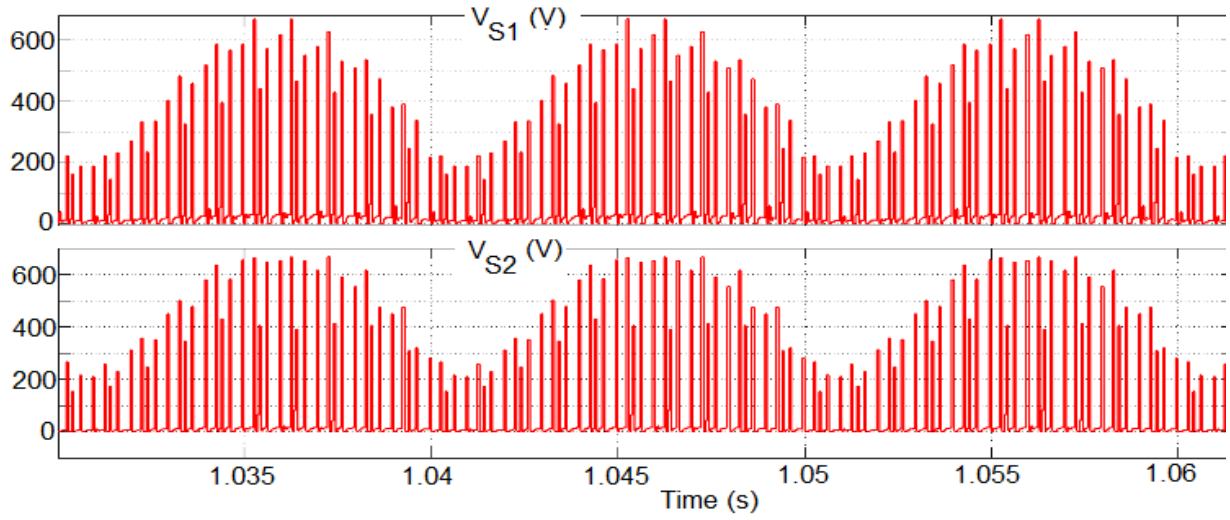


Figure 14. Voltage stresses across the switches S_1 and S_2 .

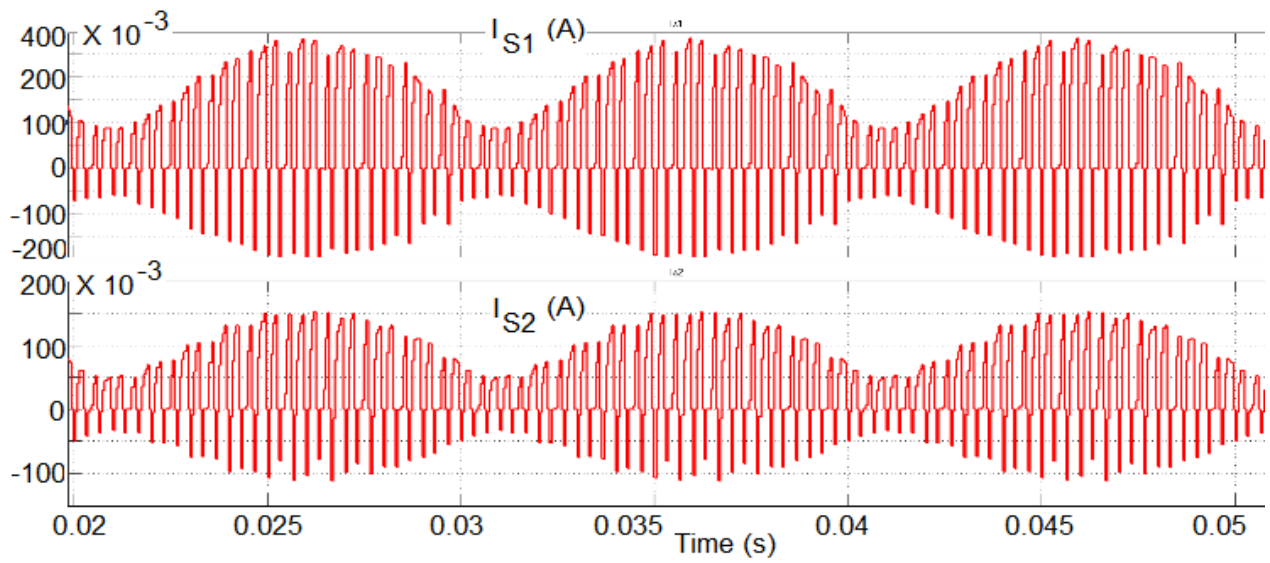


Figure 15. Currents through the switches S_1 and S_2 .

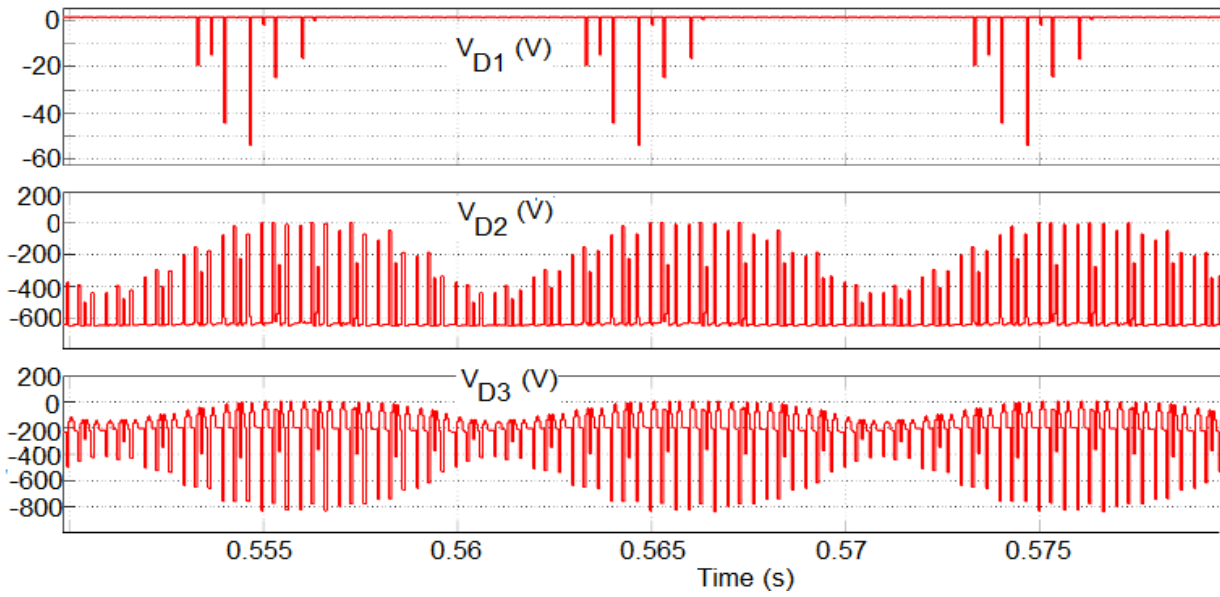


Figure 16. Voltages across the diodes D_1 , D_2 , and D_3 .

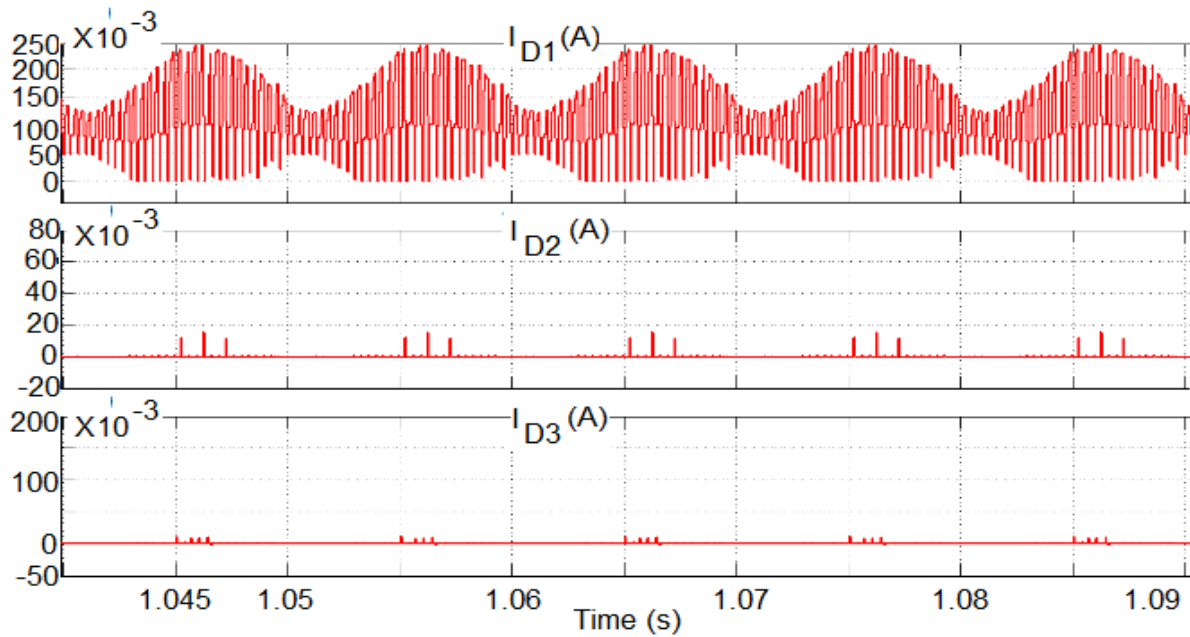


Figure 17. Currents through the diodes D_1 , D_2 , and D_3 .

4. Conclusion

In this article, the open-loop implementation of a rectifier-fed non-isolated positive output high step-up gain power electronic converter has been proposed. The high output voltage level is obtained by a parallel-charge and series-discharge inductor-based voltage boosting technique. The principle of operation and steady state analysis of the proposed converter under continuous inductor current mode operation is analyzed. Both the steady state analysis and state-space analysis of the suggested converter are carried out. The performance of the rectifier-fed DC-DC converter is validated through the time-domain simulations carried out in Matlab/Simulink platform. The results demonstrate that the rectifier-fed converter configuration proposed in this work has the capability to produce an output DC voltage of around 900 V which is almost ten times the average input DC voltage. This improved output voltage level is obtained at extremely low duty ratio of the active switches. The output voltage and output current waveforms are characterized by significantly reduced overshoot and settling time. The voltages across and the currents through the non-dissipative elements in the converter configuration are also analyzed. The proposed converter configuration employs only two high power semiconductor switches (MOSFETs). There is a considerable reduction in the voltage and current stresses for the MOSFETs. The proposed step-up converter may find applications in many real time applications such as battery backup for uninterruptible power supplies, solar cell energy conversion system, automobiles, micro-ovens, and X-ray machines and CT scanners.

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